# TrueMask® MDP

## FULL-CHIP, MODEL-BASED MASK DATA PREPARATION

The increasing complexity in mask designs—in particular the sharp increase in the need for complex sub-resolution assist features (SRAFs) at 28-nm-and-below process nodes—has given rise to new challenges with mask write times (and therefore, cost) and mask quality.

D2S TrueMask MDP is the first and only full-chip, model-based mask data preparation (MB-MDP) solution for complex masks. It offers fully automated, full-chip mask data preparation for any complex mask—including Manhattanized, curvilinear and ideal inverse lithography technology (ILT) mask shapes—within practical, cost-effective write times. TrueMask MDP reduces eBeam shot count to cut mask write times by 20-30% or more, while improving the quality of the eventual wafers through built-in mask process correction (MPC).

## PHYSICS DRIVES MASK COMPLEXITY AND COST

Optical lithography is approaching its limits with process technologies below the 28-nm node. Advanced optical proximity correction (OPC) and ILT have helped to extend the use of current 193nm with immersion (193i) lithography. But these and other techniques to improve the resolution of optical lithography can contribute to the other limiting issue: mask-write time.

To preserve wafer accuracy, main mask features that print on the wafer need to be more complex. In addition, SRAFs—mask features that help preserve depth of focus (DOF), exposure latitude (EL) and critical dimension uniformity (CDU) for the main feature they support, but which do not print themselves—also must be increasingly complex.

Conventional, rule-based fracturing is constrained to fracture the input shape into rectangular variable-shaped beam (VSB) shots, inherently limiting conventional fracturing to “Manhattanized” shapes. In the limited cases where the target shapes are curvilinear, the shape is “stair stepped” within a Manhattan grid. These Manhattan stair-steps have become smaller and smaller to achieve the best results for wafer printing. The finer the stair-step, the more eBeam shots are required to write the masks, which increases mask write times and, therefore, mask costs.

**BENEFITS:**

- Ability to deploy ideal ILT shapes for superior wafer quality
- >20-30% write-time reduction for conventional Manhattanized OPC shapes
- >50% write time reduction for ideal ILT shapes over conventionally fractured, Manhattanized ILT shapes, with superior wafer quality
- Built-in model-based MPC to improve mask linearity and CDU, particularly for small patterns, for both ArF and EUV masks
- Automatic full-chip mask verification and correction

## TRUEMASK MDP: A NEW APPROACH TO MASK DATA PREPARATION

TrueMask MDP uses mask simulation to employ overlapping, dose-modulated shots to write any desired mask contour more accurately, with fewer shots and therefore less write-time. The GPU-accelerated D2S Computational Design Platform (CDP) enables TrueMask MDP to simulate the full mask plane with 0.1-nm resolution. The shot lists output by TrueMask MDP work with the leading-edge mask writers. On VSB machines, these shots will fracture to the physical shots. On multi-beam machines, these shots will be converted to the pixel dose information on the mask writer. TrueMask MDP provides a seamless flow for data preparation, shot synthesis, data output for mask writers and inspection machines, and verification of complex masks with either Manhattanized or curvilinear target mask features.

Until now, computing an eBeam shot list based on simulation was not possible on a full-chip level because of the massive computing power required to perform these complex simulations. The >400 TFLOPS processing speed of the standard D2S CDP enables full-chip simulation in practical production timeframes. TrueMask MDP produces the shot list at a rate of 80-300B shots/day, depending on the system configuration. Full-chip data for a typical system-on-chip (SOC) with 1600 $mm^2$ mask dimensions and with a shot density of ~50 shots/$\mu m^2$ (without exploiting shape hierarchy and repetition) is processed in 24 hours or less on the standard D2S CDP.

## REDUCES WRITE TIME, IMPROVES QUALITY

TrueMask MDP is the first and only MB-MDP solution that can simulate full-chip design data using not only Manhattan data, but also ideal ILT shapes—including curvilinear shapes—fast enough to be practical for production chips. Functionality traditionally assigned to MPC can be included as a natural part of the MB-MDP process, reducing the processing steps required for data preparation of both advanced ArF and EUV masks. For example, for EUV masks, mid-range scatter of 1-2µm is included in the model and is corrected for during MB-MDP. SRAFs in ArF masks and main features in EUV masks are often sub-80nm in width; these sub-80nm features are corrected for linearity. TrueMask MDP to process mask data for critical layers confers important advantages over using only conventional fracturing for all mask layers (see figure 1).

| | Conventional Fracturing Only | Plus Rule-Based MPC | Plus Model-Based MPC | TrueMask MDP |
|---|---|---|---|---|
| Overlapping shots | ✖ | ✖ | ✖ | ✔ |
| Dose modulation | ✖ | ✔ | ✔ | ✔ |
| Ideal ILT masks | ✖ | ✖ | ✖ | ✔ |
| Full-chip mask simulation | ✖ | ✖ | ✔ | ✔ |
| EUV correction | ✖ | ✖ | ✔ | ✔ |

Figure 1. Using TrueMask MDP to process mask data for critical layers confers important advantages over using only conventional fracturing for all mask layers.

## FEATURES

- TrueModel technology enables fast, accurate full-chip modeling of complex mask shapes, including ideal ILT shapes
  - Automated calibration for a variety of effects including eBeam, resist diffusion, development, bake and etch
  - Accurate, full-chip mask simulation
- D2S Computational Design Platform >400 TFLOPS supercomputing enables full-chip processing in a day
- D2S Computational Design Platform offers redundancy and automatic recovery for 24/7 operations
  - Priority queue management for operations
- Robust visualization
- Accepts either Manhattanized data or ideal ILT shapes as input
- Outputs various writer formats, including those for die-to-database inspection

Using Manhattan shapes as input, TrueMask MDP reduces mask write times by 20-30% or more over conventional fracturing. In addition, the resulting masks have better CDU, particularly for small shapes because MPC is naturally a part of MB-MDP.

TrueMask MDP also enables the use of ideal ILT shapes in practical time frames. When compared to conventionally fractured, Manhattanized versions of ILT shapes for the same wafer target, TrueMask MDP reduces mask write times by more than 50% for these types of designs. Ideal ILT masks written with TrueMask MDP also produce wafers of a quality significantly superior to those produced by the Manhattanized ILT masks written with conventional fracturing solutions[1].

## TRUEMODEL: SIMULATING MASK SHAPES IN THEIR FULL-CHIP CONTEXT

For today's complex chips, "bundled corner-rounding models" are no longer sufficient to model mask effects. At the heart of TrueMask MDP is the D2S TrueModel® technology. The TrueModel technology includes a comprehensive mask-process model that encompasses short, medium and long-range eBeam effects, as well as mask-process effects from develop, bake and etch.

TrueModel technology models each shape in its own unique full-chip context, producing masks of a higher quality in terms of both CDU and mean-to-target (MTT), even for advanced nodes at 20nm and below.

Uniquely, TrueModel technology is able to model and configure eBeam shots to create ideal ILT shapes, which have been shown to improve mask quality and decrease eBeam shot count. In addition, TrueModel can take into account the effects of overlapping shots and eBeam dose modulation, both of which are important emerging techniques for maintaining mask CDU for advanced process nodes.

TrueModel technology includes a proprietary test chip designed to extract overlapping-shot and dose-modulation effects, and an automated model-calibration engine. The D2S CDP enables full-chip processing in a practical timeframe.

1 – "Optimization of mask shot count using MB-MDP and lithography simulation," BACUS 2011, GLOBALFOUNDRIES and D2S

## D2S COMPUTATIONAL DESIGN PLATFORM SPECIFICATIONS/SYSTEM REQUIREMENTS

- >400 TFLOPS performance
- 4 TB RAM
- 22 TB parallel file system connected to computing nodes with high-performance, internal-cluster network
- Remote GUI-based console for job submission, job-status query and hardware-status query
- High-availability features:
  - RAID 1, 5 and 6 disk configurations
  - "Running spare" computation nodes
  - Redundant master nodes
  - Redundant switches and paths in internal InfiniBand™ fabric
  - Dual power supplies for critical nodes
  - MTBF-HW > 2000 Hours
  - MTBF-SW > 200 Hours
  - Availability > 90%

## FULLY AUTOMATED SHOT SYNTHESIS IN A SIMPLE FLOW

TrueMask MDP embeds the TrueModel technology in a simple, reliable, batch-process flow. This powerful, automated shot synthesis flow (see figure 2) takes in Manhattanized or ideal ILT data and partitions the data for processing by the D2S CDP. For each partition, the TrueModel technology uses its unique, context-sensitive models to simulate the effects of all shots for opportunities to improve shot count, mask quality or both, and then synthesizes precise shot configurations based on this analysis. Finally, the partitions are assembled and fully verified before the full-chip mask data is output.

The job queue management capabilities included in the D2S CDP give users flexible control over the batch processes, such as the ability to insert a higher priority job without aborting the running jobs and to detect and automatically recover from failed nodes.

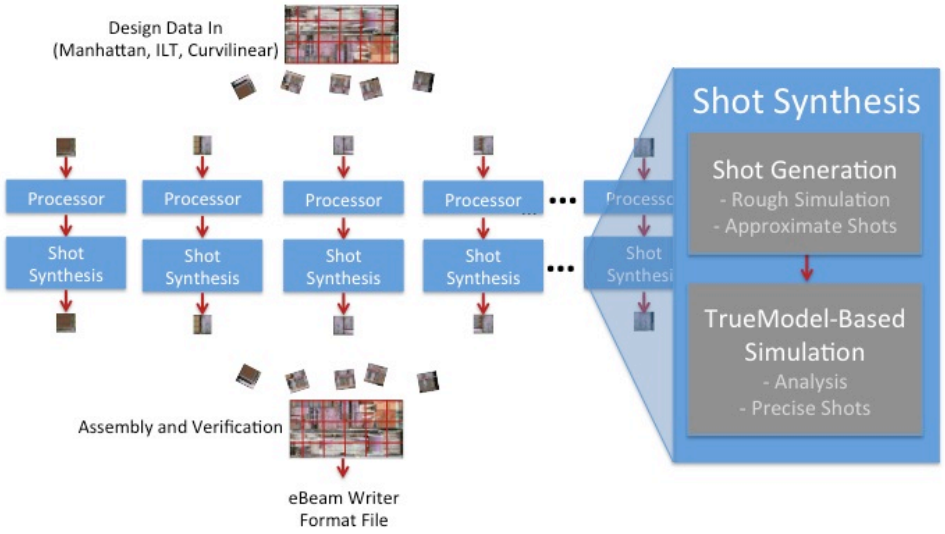


Figure 2. TrueMask MDP shot synthesis flow.

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## ROBUST VISUALIZATION FOR EVERY STEP

TrueMask MDP includes D2S TrueMask DS mask-wafer double simulation to enable users to visualize the simulated contour shapes, from the fractured design shape to the exposed resist, to an overlay of the lithography aerial image that would be projected on the wafer (see figure 3).

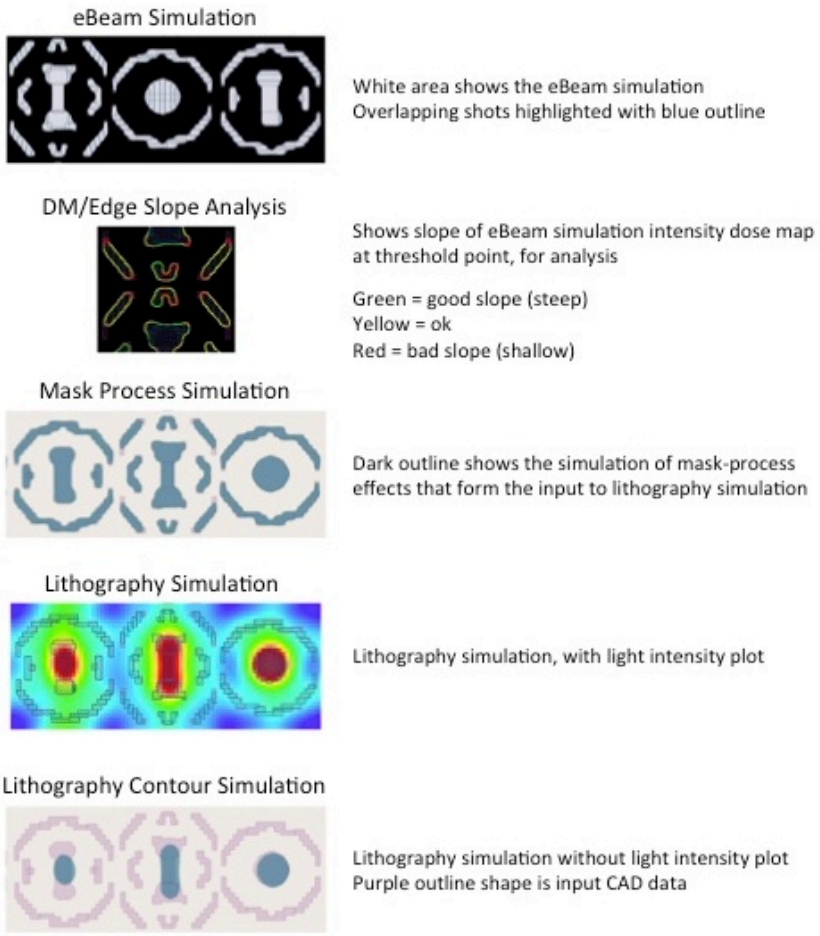


Figure 3. TrueMask MDP includes interactive visualization and analysis of eBeam shot data, DM/edge slope, mask-process simulation, and lithography simulation.