TrueMask® DS

MASK-WAFER DOUBLE SIMULATION ACCELERATED WORKSTATION

As the size of mask features moves into the sub-80nm realm, mask accuracy has become an increasingly difficult problem with increasing impact on wafer yield. D2S TrueMask DS accelerated workstation is the first and only mask-wafer double simulation platform for R&D exploration, bit-cell design, hot-spot analysis, and mask-defect categorization that comprehends overlapping shots and dose modulation.

BENEFITS:

- Interactive visualization of the impact of a change in mask shapes in the wafer plane.
- Interactive optimization of mask shot-count and wafer quality using the benefits of overlapping shots and dose modulation
- Interactive visualization for hot-spot and failure analysis, as well as for process development
- Productivity gains for mask model calibration and exploration during process development

Additionally for memory cells:

- Improved wafer yield
- Improved throughput for mask production through reduced mask shot-count

MASK SIMULATION IS REQUIRED FOR 28-NM AND BELOW

Optical-process correction (OPC) technologies add sub-resolution-assist features (SRAFs) to compensate for the optical effects that prevent fine features from printing correctly. Particularly at the 28-nm-and-below nodes, the shapes of SRAFs – and even main features – need to become more complex to produce the desired images with sufficient process window on the wafer. Multiple patterning and "regular design rules" need to be coupled with complex OPC technologies. However, with all this added data, mask write-times will explode, making necessary engineering trade-offs between acceptable wafer accuracy and tolerable mask-write times.

Simultaneously, as the sizes of the majority of the shapes on the mask become smaller than 80-nm, a new problem has emerged: shapes output by OPC no longer faithfully reproduce on the mask. Due to the radius of the combined short-range blur from the eBeam used to write masks plus the mask-process effects from develop, bake, and etch processes, a 60-nm square feature, as an example, does not print as a square, but as a smaller-sized circle with poor dose margin (DM), as shown in Figure 1 (below). As the industry ramps up for the 14-nm process node and below, this becomes an issue for main features as well. Intervention is required to correct the inaccuracy and the poor tolerance to manufacturing variation of smaller features.

The only definitive way to gain insight into these issues without test printing is mask-wafer double simulation.

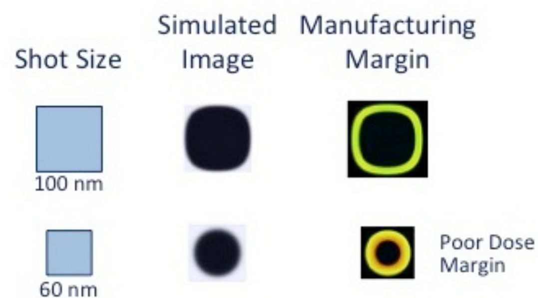

Figure 1. Features smaller than 80nm do not print as intended, even with eBeam, and have poor DM.

FEATURES

- 0.1nm resolution mask simulation up to 300µm x 300µm (mask dimensions), including overlapping shots and dose modulation:
  - Instantaneous eBeam simulation using hardware acceleration
  - eBeam simulation of contours, contour differences, and DMs
  - Mask process (develop, bake, and etch) simulation
- Advanced eBeam modeling with arbitrary point-spread functions for exploration
- Fast, interactive aerial lithography simulation using hardware acceleration
- Aerial lithography simulation of ArF with various light sources and EUV
- 5µm x 5µm (on wafer) interactive mask-wafer double simulation
- SEM interface for overlay analysis of pictures with simulations
- Inputs: GDSII and OASIS formats
- Outputs: GDSII, VSB-12 and JEOL formats
- TCL-based extension language for user customization

TRUEMASK DS ENABLES BETTER MASKS, INFORMS TRADE-OFFS

TrueMask DS provides the industry's only mask-wafer double-simulation platform for accurate analysis of wafers written with masks that contain sub-80nm features, and/or deploy overlapping shots or dose-modulation for DM improvement. When "bundled corner-rounding models" are no longer sufficient to model mask effects, double simulation – including mask-process simulation for develop, bake, and etch effects – is the only way to physically model the effects on wafer. Mask-wafer double simulation is also the only way to explore the trade-offs between mask effects, particularly between mask shot-count (and therefore write-times), and wafer quality.

By deploying hardware acceleration, the double simulation is accomplished for 5µm x 5µm (on wafer) areas at interactive speeds. Users can experiment using different variable-shaped beam (VSB) shots to write masks, optionally using overlapping shots and dose modulation, and instantly see the contour shape of the exposed resist, then within seconds see an overlay of the lithography aerial image that would be projected on the wafer.

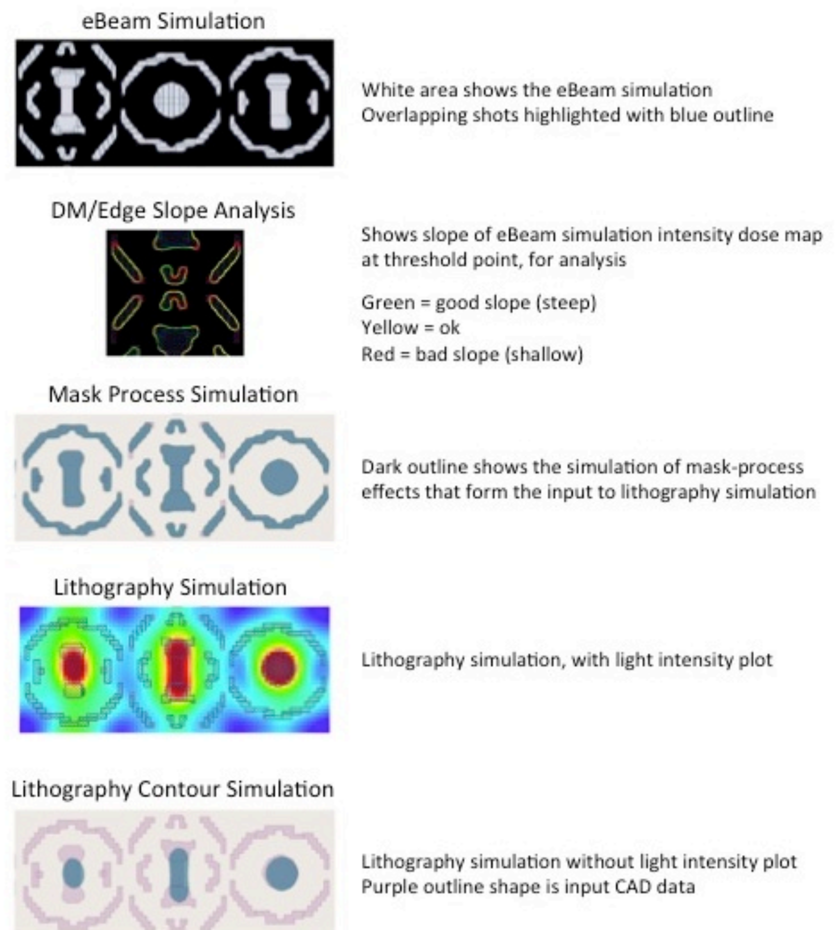

Figure 2. TrueMask DS enables interactive visualization and analysis of eBeam shot data, DM/edge slope, mask-process simulation, and lithography simulation.

SPECIFICATIONS/SYSTEM REQUIREMENTS

TrueMask DS is a complete mask-wafer double simulation acceleration workstation. The workstation is comprised of a dual-GPU, desk-side, air-cooled, computer with dual large-screen monitors, keyboard and mouse. The 2-teraFLOPS computer has 128 GB internal memory. TrueMask DS mask-wafer double simulation software pre-installed. For use in typical, air-conditioned, ambient temperatures without additional cooling.

TRUEMASK DS MASK-WAFER DOUBLE SIMULATION APPLICATIONS

TrueMask DS is an integrated platform for the design and analysis of a mask clip with visualization both in the mask plane and in the wafer plane. This capability is valuable through many phases of design to manufacturing, and can be useful for mask engineers, product engineers, OPC engineers, memory-cell designers, and test-chip engineers.

Mask Engineer

When OPC output shapes are smaller than 80-nm, and particularly when the resulting mask shapes are not written with axis-parallel edges of VSB shots, mask shapes can only be predicted through simulation. Mask engineers must also evaluate and optimize tolerance to mask manufacturing variation, such as indicated by dose margin, for these shapes. Particularly for highly repetitive patterns and for critical areas, mask engineers need to explore alternative shot configurations. When comparing two alternative shot configurations, the ultimate test is a comparison in the wafer plane of the two designs, each with full eBeam simulation followed by mask process simulation, and then by aerial lithography simulation. Only TrueMask DS can give mask engineers this comprehensive comparison.

Product Engineer

TrueMask DS is a valuable tool for post-analysis of product-engineering issues. Hotspot analysis of wafer defects or yield problems requires a study of wafer processing, mask processing, and OPC. TrueMask DS is the only tool that includes both eBeam and optical models, identifying hotspots due to both mask and wafer manufacturing process variations. Product engineers can overlay mask and wafer scanning electron microscope (SEM) photographs on top of simulation results to pinpoint problems.

OPC Engineer

OPC engineers are focused on obtaining the best wafer yield possible within a reasonable mask-write time. TrueMask DS offers OPC engineers the unique ability to explore trade-offs between wafer quality and mask-write times quickly. For sub-28-nm-node designs, SRAFs and other decorations are often sub-60-nm in width. These features suffer from significant degradation on mask, even before wafer effects come into play. Rule-based approaches cannot predict the interactions between neighboring shapes. The fast, accurate eBeam and mask process simulations that form the input data into the fast lithography simulation in TrueMask DS is the only way to predict accurately the impact of mask-shape variation on the wafer. At 28-nm, DM on the mask starts to play a significant role on the wafer process window and critical-dimension uniformity (CDU). In addition, with the use of overlapping shots and dose modulation, more ideal inverse lithography technology (ILT) masks can be deployed without increasing mask-write times.

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7,745,078; 7,754,401; 7,759,026; 7,759,027;
7,799,489; 7,901,845; 7,901,850; 7,981,575;
8,017,286; 8,017,288; 8,017,289
Additional patents pending.

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TRUEMASK DS APPLICATIONS, CONT.

Memory Cell Designer

The design of any highly critical circuit deserves more careful attention. A small change in the design can have a high impact on wafer yield. TrueMask DS enables circuit designers to design with mask VSB shots as the units of operation, rather than drawing polygons. Taking advantage of overlapping shots and dose modulation, the circuit designer can create curvilinear mask shapes that create superior wafer performance while at the same time improving DM on the mask for better CDU on mask and wafer. The TrueMask DS mask-wafer double simulation platform enables circuit designers for the first time to simultaneously design the mask shots, the mask shapes, and the wafer shapes in interactive time. Because it is simulation-based, TrueMask DS enables cell designers to explore mask shapes that may violate mask design rules but can, in fact, be reliably manufactured with reasonable mask-write times.

Memory cells are not only critical circuits, but also highly repeated shapes. One VSB shot saved or added in writing a memory cell has a substantial impact on mask-write times and therefore on cost and turnaround time for every design that uses that circuit. In the ultimate design-to-manufacturing integration, circuit designers are able to dictate exactly the trade-off between mask-write times and impact on wafer yield by using TrueMask DS.

Test Chip Engineer

TrueMask DS offers an integration platform on which to design test chips that include overlapped and dose-modulated VSB shots, to simulate and analyze expected results, and to evaluate SEM results for model matching. CD markers can be exported to SEM, and SEM pictures can be imported into TrueMask DS through comma-separated value (.csv) interfaces to assess model fit quickly.