Agency Contact:
David Moreno
MCA
Tel: +1-650-968-8900, ext. 125
E-mail: dmoreno@mcapr.com

D2S UNVEILS FIFTH-GENERATION GPU ACCELERATION PLATFORM FOR SEMICONDUCTOR MANUFACTURING

Latest-generation Computational Design Platform more than doubles processing speed and enables the first inline dose correction in multi-beam mask writers

SAN JOSE, Calif., April 4, 2017—D2S®, a supplier of GPU-accelerated solutions for semiconductor manufacturing, today announced the unveiling of the fifth generation of its computational design platform (CDP), which enables extremely fast and precise simulations for semiconductor design and manufacturing. Featuring NVIDIA Pascal-based Tesla P40 GPUs, the fifth-generation CDP achieves 888 Teraflops of processing speed—more than twice as fast as the previous-generation CDP from D2S. The first two units of the fifth-generation CDP will be delivered by the end of the second calendar quarter of 2017, bringing the total number of CDPs across all five platform generations installed worldwide to 20—representing more than five Peta-FLOPs of computing power. CDPs are architected to ensure the high speed, precision and reliability required for 24x7 cleanroom production environments.

"Seismic changes are underway in the photomask and semiconductor industry, prompting the need for greater simulation capability," stated Aki Fujimura, CEO of D2S. "Inverse lithography technology (ILT) and complex mask shapes, which are already being utilized in some leading-edge chip designs, will be increasingly needed as the industry migrates to smaller design nodes. Significant progress is being made with multi-beam mask writing, which provides write times that are independent of shape count or complexity—making it ideal for these complex features. Progress also continues on EUV mask development, which will require extreme mask writing precision as well as high shape counts. However, with all of these major technology transitions, the computational power required to precisely simulate the physical effects of photomask designs and semiconductor processes will skyrocket—driving the need for GPU acceleration to enable simulation-based processing in reasonable run times."

-more-

A white paper on the benefits of GPU acceleration is available for download at www.design2silicon.com/download_gpu_whitepaper.

The D2S CDP is an extremely powerful processing solution that can simulate the entire mask plane (1.4 quintillion pixels). It is engineered for high reliability, redundancy and recovery to support stringent environmental requirements, and fully conforms with SEMI S2. The water-cooled CDP design is optimized for cleanroom manufacturing environments.

The newest application for the D2S CDP is inline linearity correction for multi-beam mask writing, which provides pixel-level dose correction to enhance the printability of masks incorporating more complex and smaller features. A summary of the current semiconductor manufacturing applications where D2S GPU-accelerated CDPs are being used include:

- model-based mask data preparation (MB-MDP) for designing leading-edge photomasks that require increasingly complex mask shapes;
- wafer plane analysis of mask images captured in scanning electron microscopy (SEM) systems to accurately identify mask problems that matter to the wafer in interactive time;
- inline thermal-effect correction of eBeam mask writers to lower write times to an acceptable level;
- geometric checking and manipulation of curvilinear shapes on masks and wafers; and
- inline linearity correction and printability enhancement for the NuFlare MBM-1000 multi-beam mask writer

“Multi-beam is an enabling technology for writing curvilinear ILT features due to its ability to handle any mask shape without loss of accuracy or speed,” stated Noriaki Nakayamada, chief specialist at NuFlare Technology. “Since curvilinear mask data correction for dose and resist effects is required to make ILT possible, implementing inline linearity correction in multi-beam machines is useful, as it eliminates the need to add an extra offline data preparation step. However, doing so is extremely compute-intensive and difficult to accomplish. D2S GPU acceleration technology makes inline linearity correction possible for the first time, which can significantly reduce turnaround time for mask processing.”

"GPUs excel at simulating natural phenomena and work well in low latency situations, making them an ideal solution for advanced semiconductor manufacturing," added Fujimura. "We're pleased to see that the industry is increasingly recognizing the benefits of GPU acceleration. For example, the Photomask Japan Symposium taking place this week in Yokohama is, for the first time, dedicating multiple sessions of its program to the use of GPUs in mask making. That's an important signal that GPU acceleration has arrived and will be a key enabler for leading-edge mask and chip designs."

D2S offers its GPU-accelerated platform as part of its TrueMask® family of products and as custom OEM additions to manufacturing systems. For more information on the Computational Design Platform from D2S, visit www.design2silicon.com/products_cdp.

D2S will present a paper co-authored with NuFlare Technology on GPU-accelerated inline linearity correction during the "Use of GPU in Mask Making II" session at the Photomask Japan 2017 Symposium on Wednesday, April 5 from 16:30 to 18:00. For more information, visit www.photomask-japan.org/.

About D2S, Inc.

D2S is a supplier of GPU-accelerated solutions for semiconductor manufacturing. The company provides simulation-based custom solutions to leading equipment partners. D2S TrueMask® solutions use the D2S Computational Design Platform to enable advanced photomask designs using complex shapes for superior wafer quality but within practical, cost-effective write-times. D2S is the managing sponsor of the eBeam Initiative. Headquartered in San Jose, Calif., the company was founded in 2007. For more information, see: www.design2silicon.com.

###