Agency Contact:
David Moreno
MCA
Tel: +1-650-968-8900, ext. 125
E-mail: dmoreno@mcapr.com

ADVANTEST AND D2S PARTNER TO TACKLE CD UNIFORMITY ERRORS WITH GPU-ACCELERATED WAFER PLANE ANALYSIS FOR ADVANCED PHOTOMASKS

Enables fast, highly repeatable and cost-effective CD metrology for complex mask shapes, including those resulting from Inverse Lithography Technology, to evaluate their impact on the wafer

SAN JOSE, Calif., **September 29, 2015**—D2S®, a supplier of GPU-enabled software for semiconductor manufacturing, today announced that **it has partnered with Advantest**, the world's largest supplier of semiconductor Automatic Test Equipment, to integrate D2S' **Wafer Plane Analysis engine** into Advantest's Mask MVM-SEM (Multi Vision Metrology Scanning Electron Microscope) systems. This new capability **enables fast and highly repeatable CD metrology for complex photomask shapes**, including those created by inverse lithography technology (ILT), which enables photomask manufacturers to quickly, accurately and cost-effectively identify mask-level CD uniformity (CDU) issues that will **impact the wafer** during subsequent lithography processing in the wafer fab.

"We're pleased to be working with D2S on developing a joint solution to improve mask CDU analysis, which results in a better quality mask for our customers," stated Takayuki Nakamura, Executive Officer, General Manager of Nanotechnology Business Division, Advantest. "Combining D2S' expertise in GPU-accelerated simulation technologies with our leading-edge CD-SEM tools—such as our new E3640—allows us to provide a cost-effective platform for extremely fast lithography simulation."

Rising Mask Complexity Requires Improved Analysis of What Matters to Wafer Yields

Advanced photomasks are increasingly adopting non-orthogonal patterns and complex shapes, such as curvilinear mask patterns, due to the need for **aggressive optical proximity correction (OPC) and ILT** in order to enable production of leading-edge semiconductor devices with ever-smaller feature sizes. As these mask patterns become more complex, conventional CD metrology that measures CDs on straight lines/spaces no longer works since most mask patterns do not have uniform CDs after OPC and ILT correction. In addition, the number of mask defect issues flagged during mask inspection increases. However, not all of these mask issues will actually result in yield problems on the wafer. As

a result, this increases the need for photomask manufacturers to understand the wafer-level impact of mask-level issues.

Wafer plane (aerial) analysis has emerged as the solution of choice for identifying mask-level CDU issues that will impact the wafer. However, optical-based wafer plane analysis solutions are expensive, can be slow to implement, and have difficulty providing repeatable results. Mask manufacturers need a new wafer plane analysis solution that is less expensive, faster, and highly repeatable without requiring new equipment or additions to the mask inspection process.

The D2S Wafer Plane Analysis Engine provides **aerial simulation of mask contours extracted by the Advantest MVM-SEM** for today's complex mask patterns, including ILT shapes for memory and logic. It is fully integrated into the Advantest CD-SEM system, which enables mask shops to access the benefits of GPU-accelerated wafer plane analysis without adding costly iterations with a standalone optical system.

"**GPU acceleration** is a powerful tool for **enabling fast and accurate aerial simulation of complex mask patterns**. It is particularly advantageous on **curvilinear mask contours**, which are increasingly being populated in today's leading-edge photomasks," stated Dr. Linyong (Leo) Pang, chief product officer and executive vice president of D2S. "The new Wafer Plane Analysis Engine from D2S provides wafer plane analysis capability **within seconds**. Combining our capability with Advantest's SEM solutions gives their customers a powerful solution for identifying which mask features truly have a CDU problem on the wafer in order to enable swift and cost-effective correction. It can also be used for mask post-inspection defect review to enable fast dispositioning of defects based on their simulated printability. "

The Wafer Plane Analysis Engine is available now from D2S. More information on the product is available at www.design2silicon.com.

About Advantest Corporation

A world-class technology company, Advantest is the leading producer of automatic test equipment (ATE) for the semiconductor industry and a premier manufacturer of measuring instruments used in the design and production of electronic instruments and systems. Its leading-edge systems and products are integrated into the most advanced semiconductor production lines in the world. The company also focuses on R&D for emerging markets that benefit from advancements in nanotech and terahertz technologies, and has introduced multi-vision metrology scanning electron microscopes essential to photomask manufacturing, as well as groundbreaking 3D imaging and analysis tools. Founded in Tokyo in 1954, Advantest established its first subsidiary in 1982, in the USA, and now has subsidiaries worldwide. More information is available at www.advantest.com.

About D2S, Inc.

D2S is a supplier of GPU-enabled software for semiconductor manufacturing. The company provides simulation-based custom solutions to leading equipment partners. D2S TrueMask® solutions use the D2S Computational Design Platform to enable advanced photomask designs using complex shapes for superior wafer quality but within practical, cost-effective write-times. D2S is the managing sponsor of the eBeam Initiative. Headquartered in San Jose, Calif., the company was founded in 2007. For more information, see: www.design2silicon.com.

###

D2S, the D2S logo and TrueMask are registered trademarks of D2S, Inc. MVM-SEM is either a registered trademark or trademark of Advantest Corporation in Japan, the United States and other countries.