



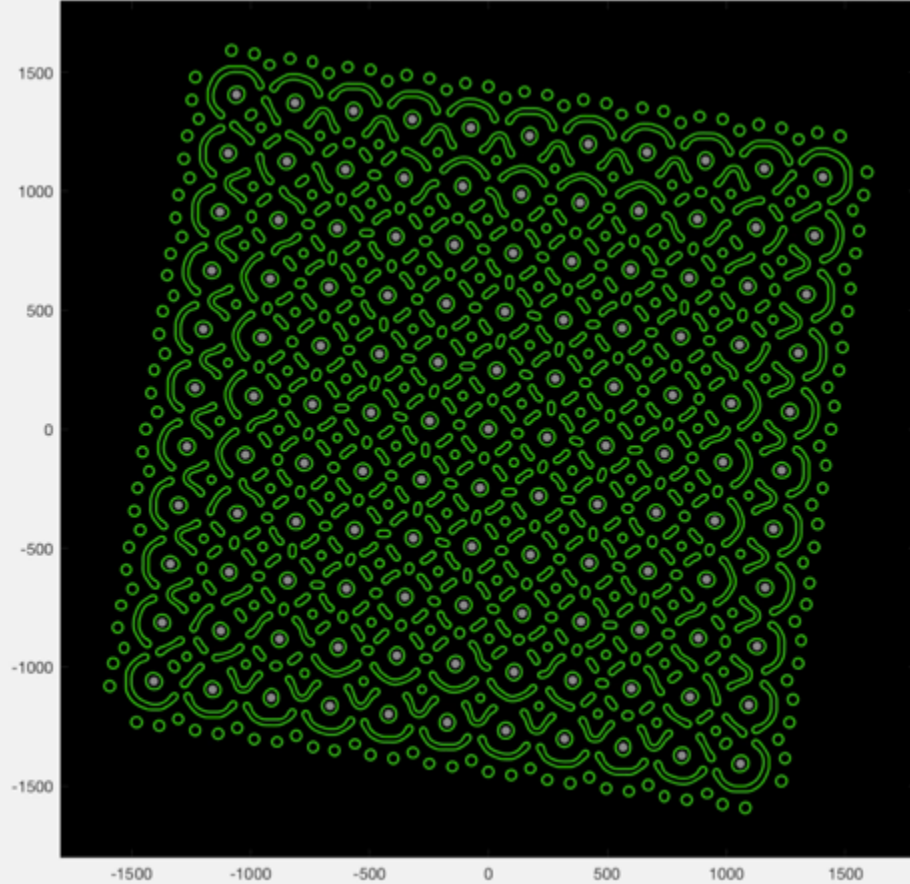
# TrueMask® ILT MWCO: Full-Chip Curvilinear ILT in a Day & Full Mask Multi-Beam and VSB Writing in 12 hours for 193i

FEBRUARY 26, 2020 | <sup>1</sup>LINYONG (LEO) PANG, PHD

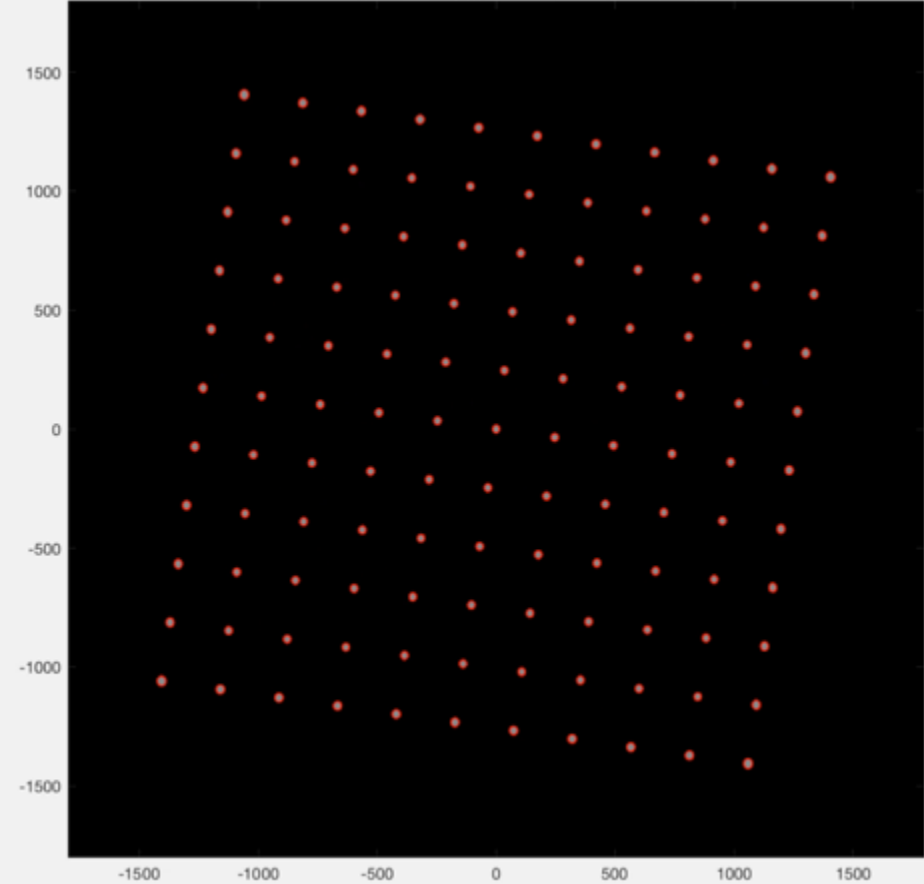
P. Jeffrey Ungar, Ali Bouaricha, Lu Sha, Michael Pomerantsev, Mariusz Niewczas, Kechang Wang,  
Bo Su, Ryan Pearman, Aki Fujimura

D2S, Inc. (US)

# Full-Chip Curvilinear ILT is Much Faster to Compute and Write with VSB Than You Think



TrueMask ILT curvilinear mask designs for different pitches & orientations



Corresponding wafer target & simulated wafer contours



# ILT with Level-Set Method Started a Decade Ago

## Fast Inverse Lithography Technology

Daniel S. Abrams, Linyong Pang

Luminescent Technologies, Inc., 650 Castro Street, Suite 220, Mountain View, CA 94041, U.S.A.





# A Different Approach based on GPU Invented by GAUDA, Extended by D2S

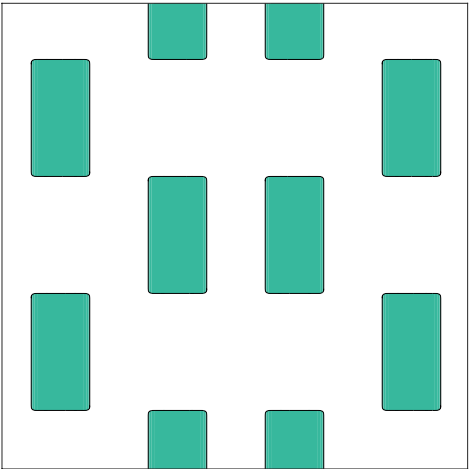


(12) **United States Patent**  
Ungar et al.

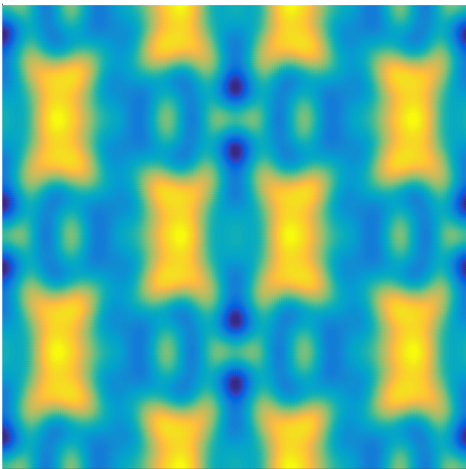
(10) **Patent No.:** US 7,856,612 B1  
(45) **Date of Patent:** Dec. 21, 2010

(54) **LITHOGRAPHY MASK DESIGN THROUGH  
MASK FUNCTIONAL OPTIMIZATION AND  
SPATIAL FREQUENCY ANALYSIS**

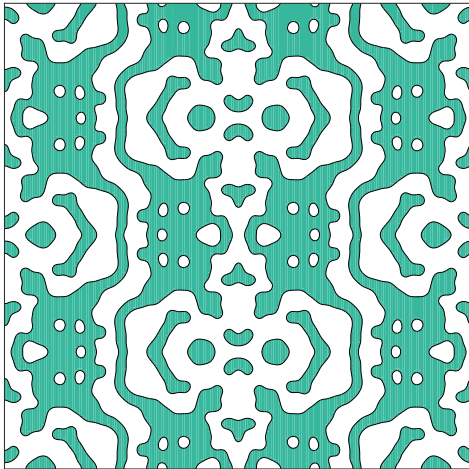
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|-----------|------|--------|----------------|---------|
| 6,611,953 | B1   | 8/2003 | Filseth et al. |         |
| 7,063,920 | B2 * | 6/2006 | Baba-Ali       | 430/5   |
| 7,266,803 | B2   | 9/2007 | Chou et al.    |         |
|           |      |        |                | 359/363 |
|           |      |        |                | 716/21  |
|           |      |        |                | 716/19  |
|           |      |        |                | 430/5   |
|           |      |        |                | 355/53  |



Target Pattern



Continuous Tone  
Fourier ILT Mask

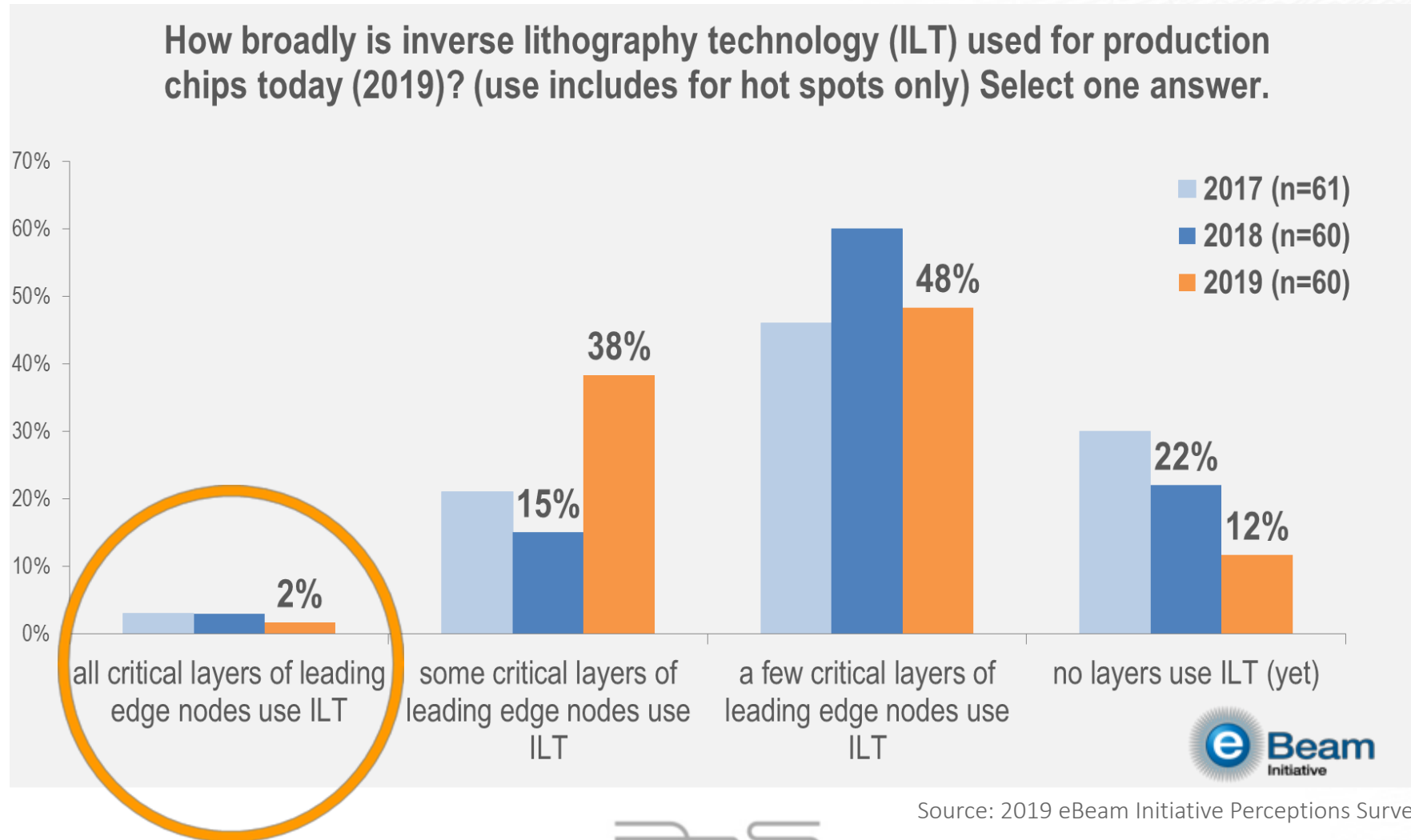


Binary Fourier  
ILT Mask



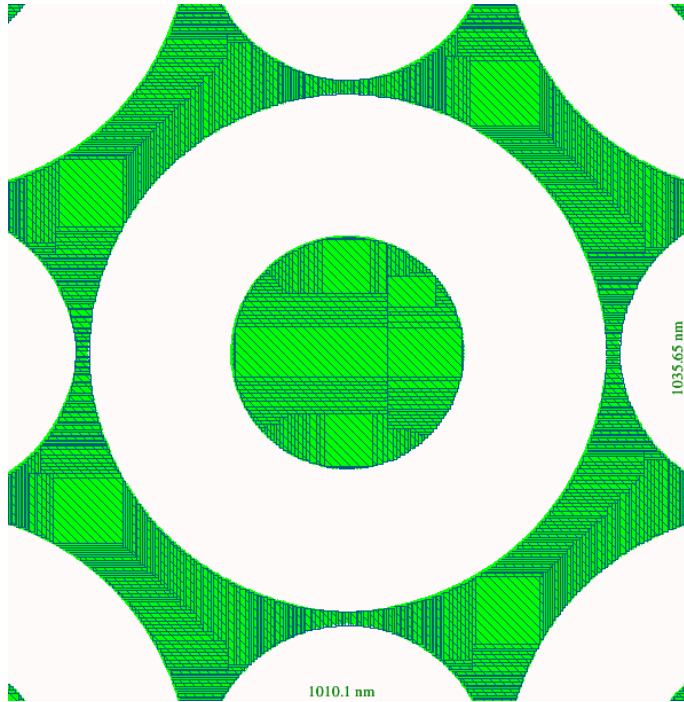


# Why isn't Curvilinear ILT Used in All Critical Layers?



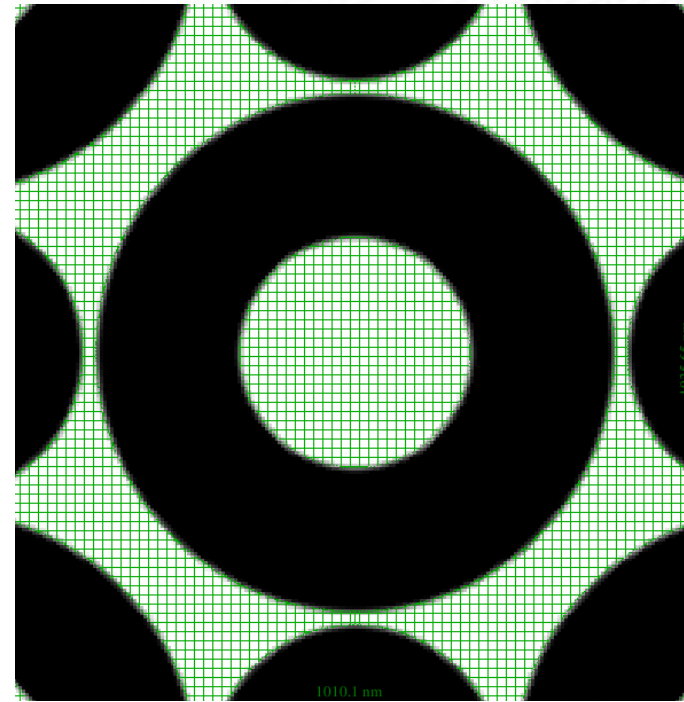
# Before: ILT Mask Write Time is Too Long

## Now: Multi-beam Mask Writers Enable Curvilinear ILT



Conventional VSB mask writer

- Generates too many shots
- Takes too long to write

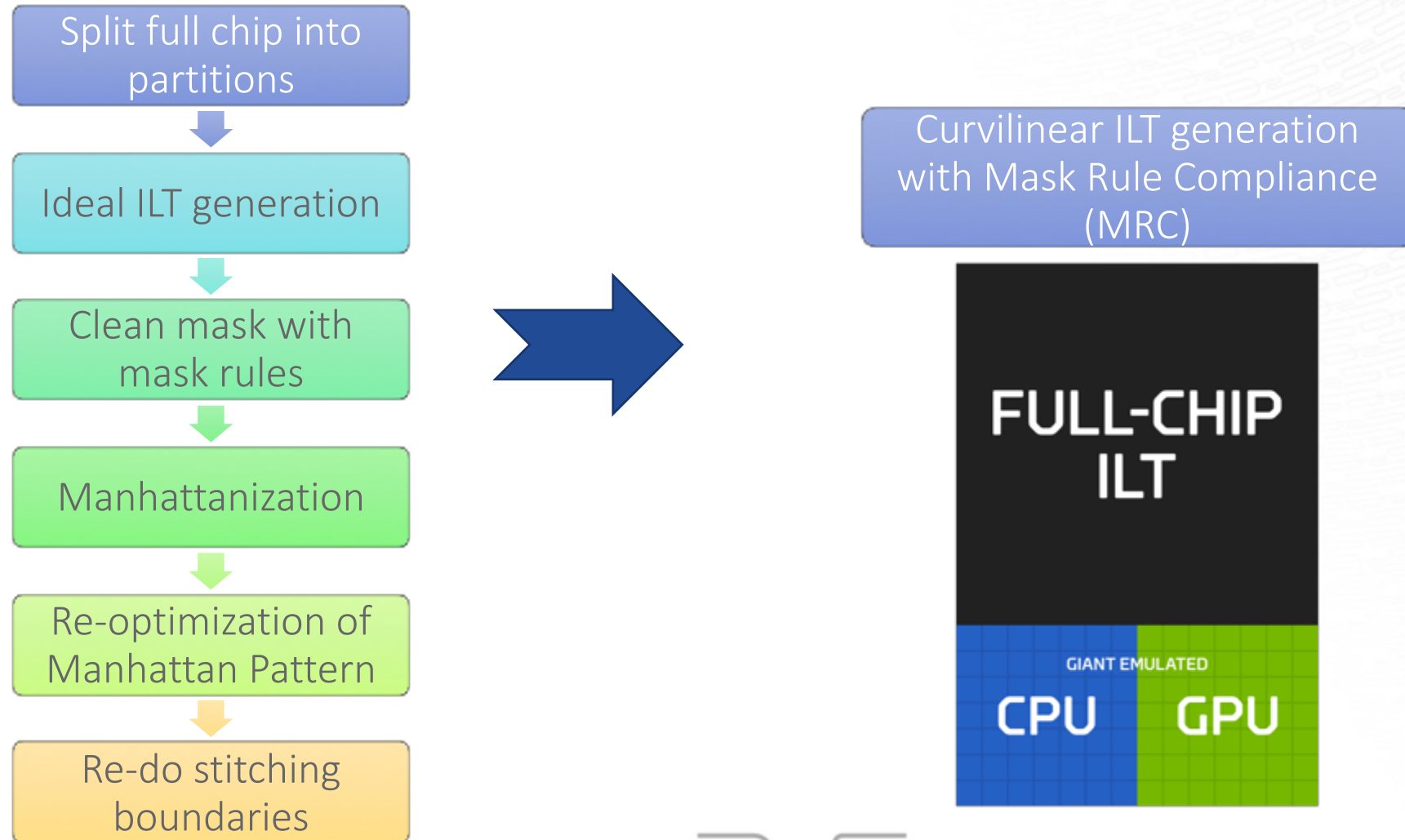


Multi-beam mask writer

- Designed for curvilinear ILT
- Writes any shape in constant time

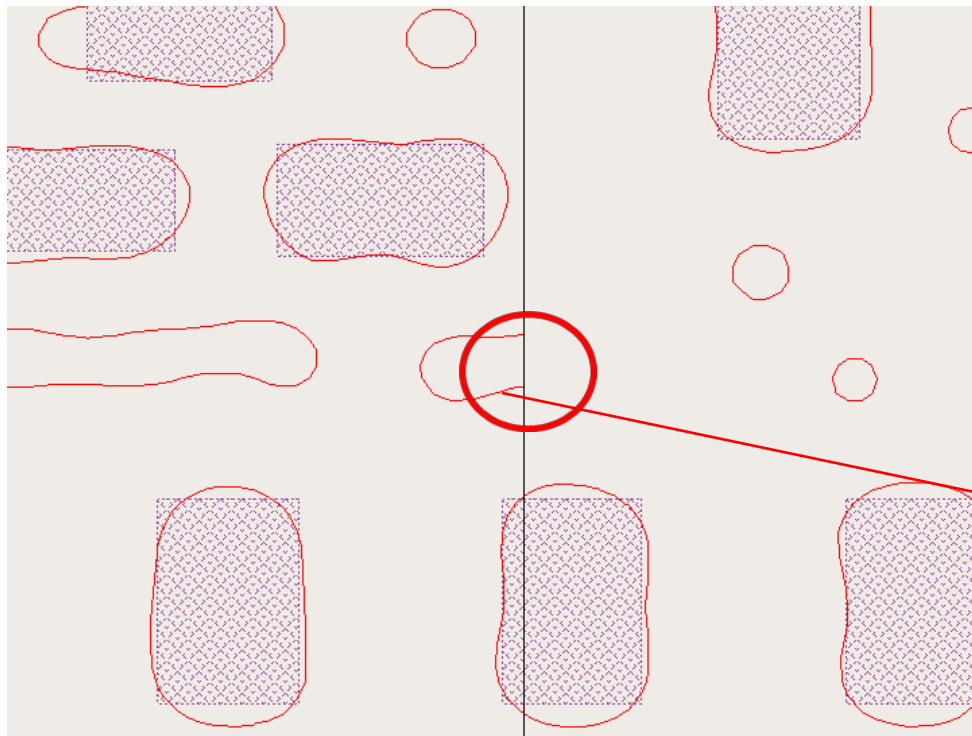
# Before: Full Chip ILT Run Time is too Long

## Now: TrueMask® ILT Solves ILT Computing Challenges



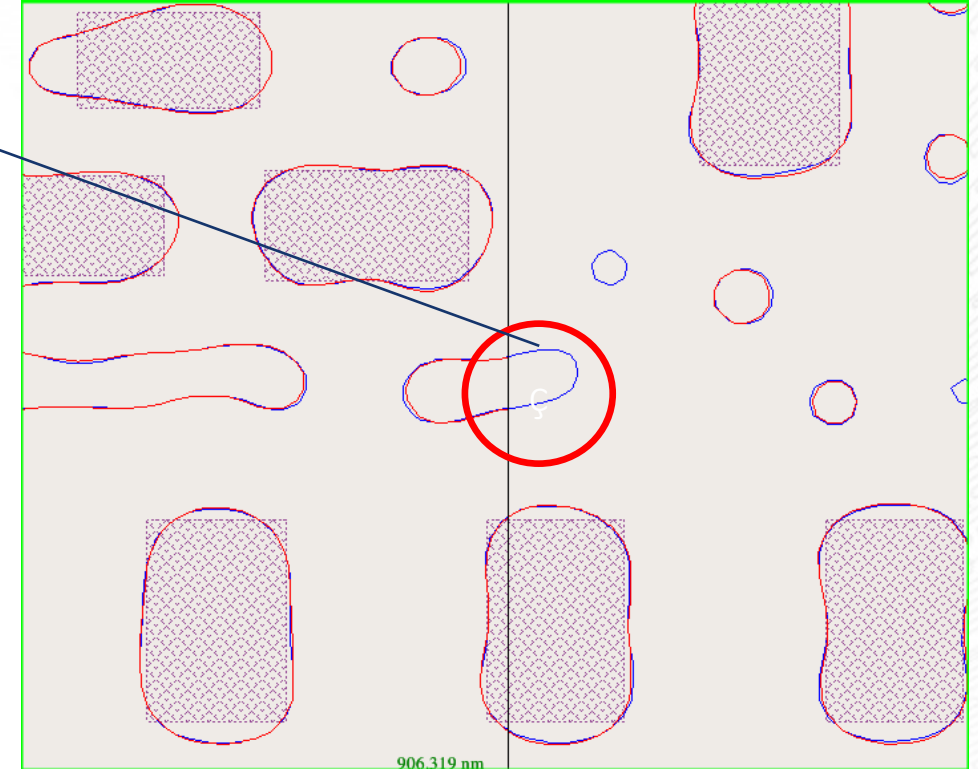


# TrueMask ILT Emulates a Giant CPU/GPU Pair: No Stitching Errors



Blue Contour:  
"Gigantic  
CPU/GPU Pair"

Red Contour:  
Partitions  
processed  
separately and  
then stitched



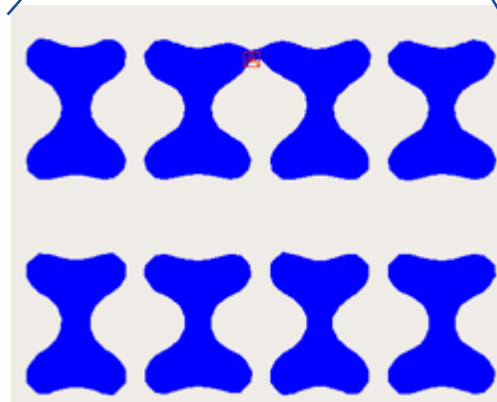
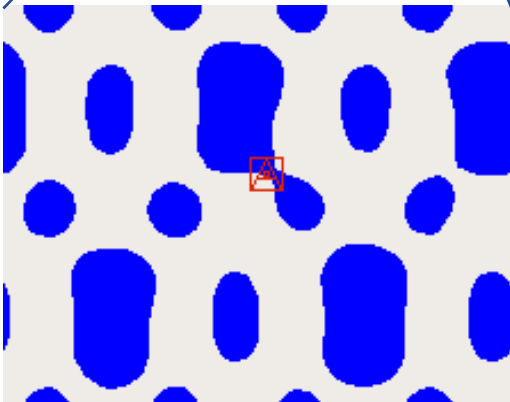
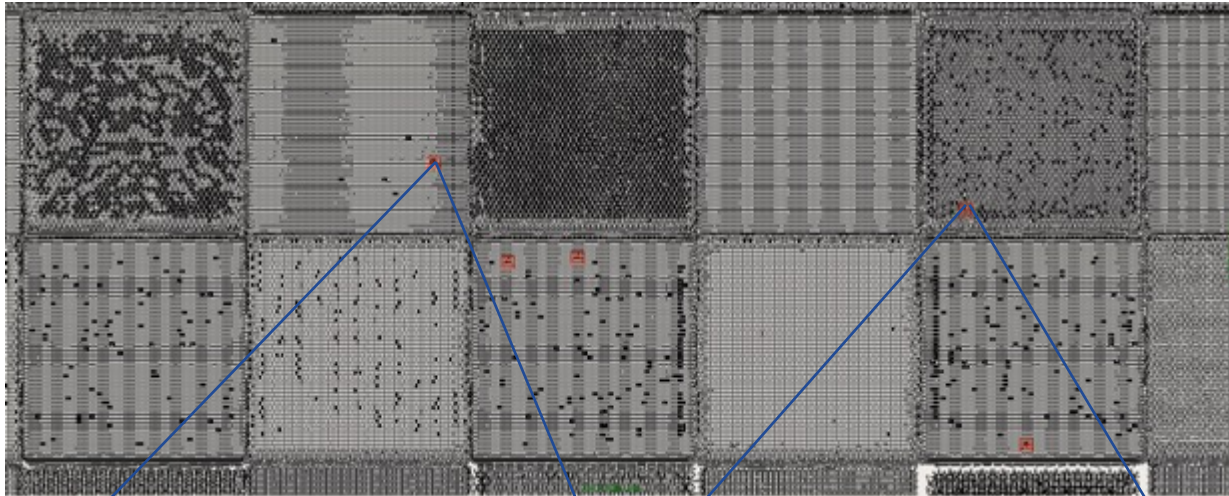
Conventional ILT: Stitching issues occur  
when partitions are putting together

TrueMask ILT: The entire chip is updated  
in each iteration, no stitching issues

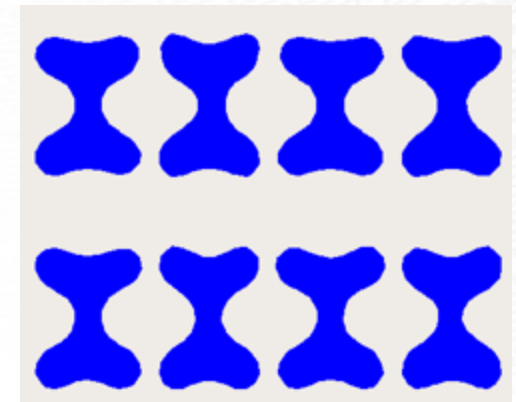
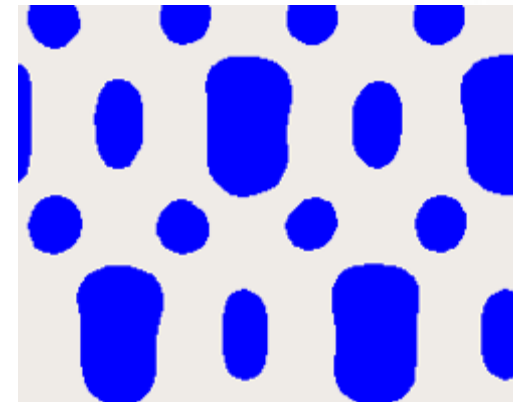
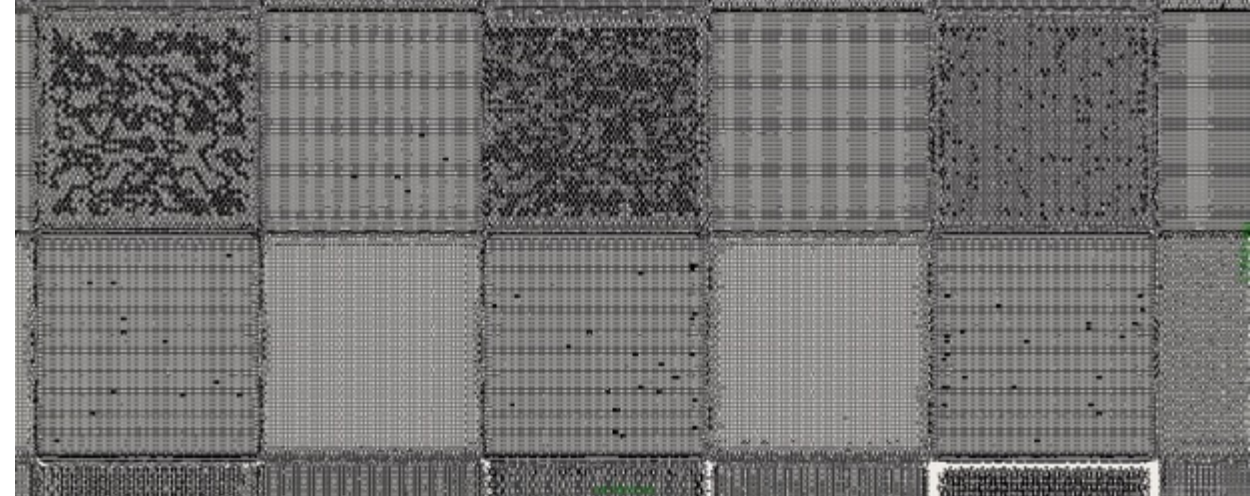


# TrueMask ILT Integrates Curvilinear Mask Rules to Produce MRC Clean Results

Without Curvilinear Mask Rules

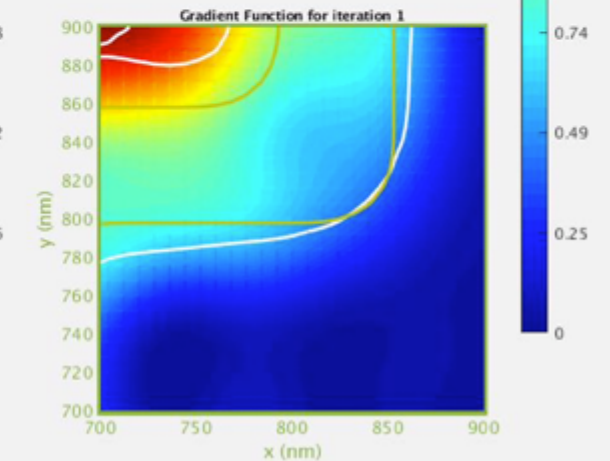
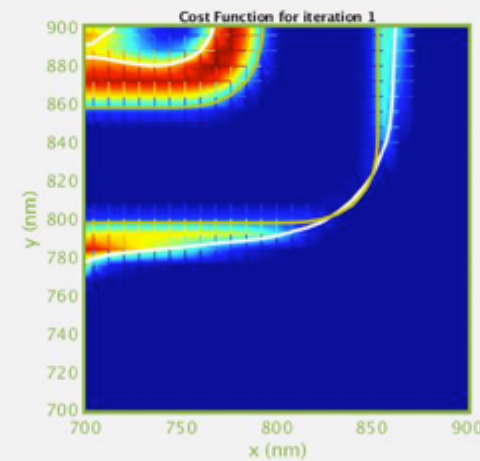
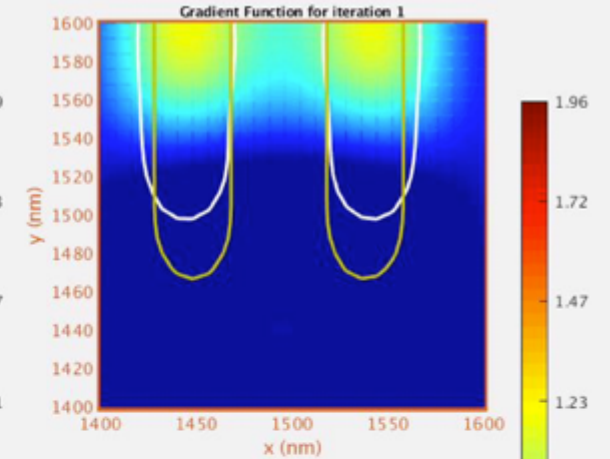
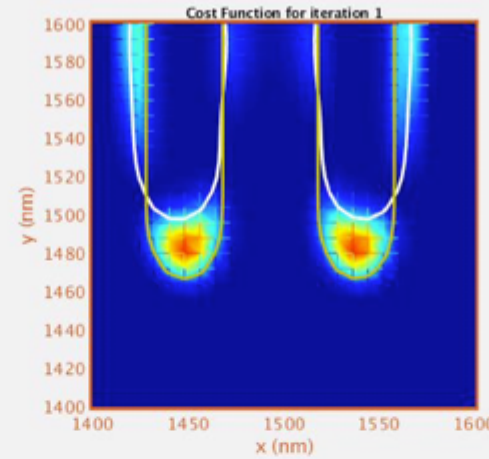
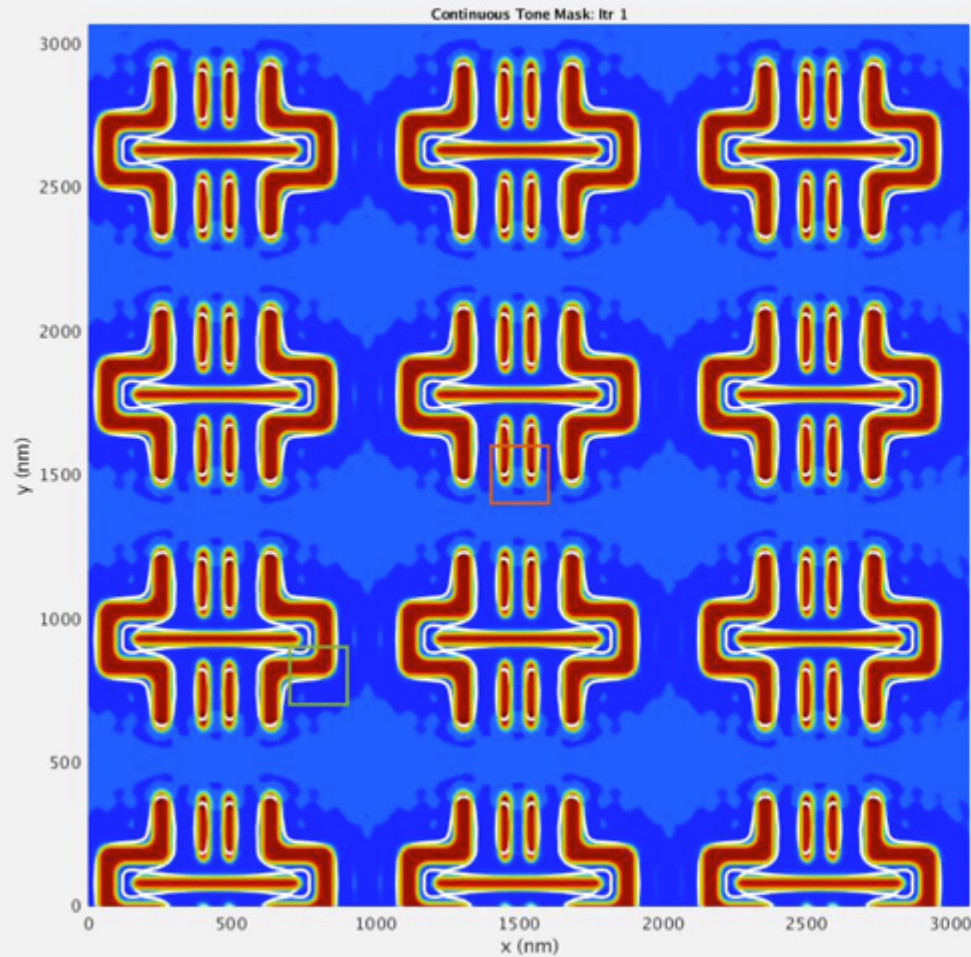


With Curvilinear Mask Rules



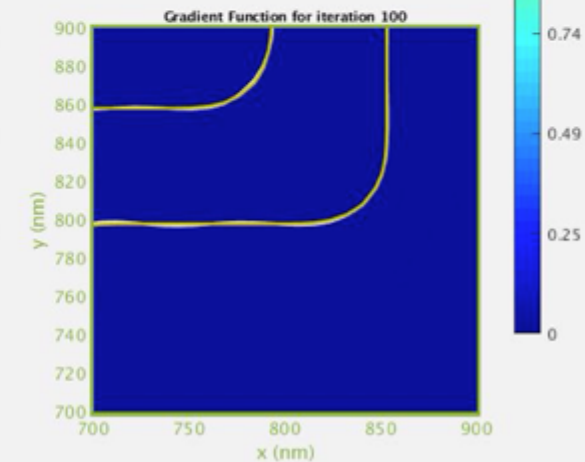
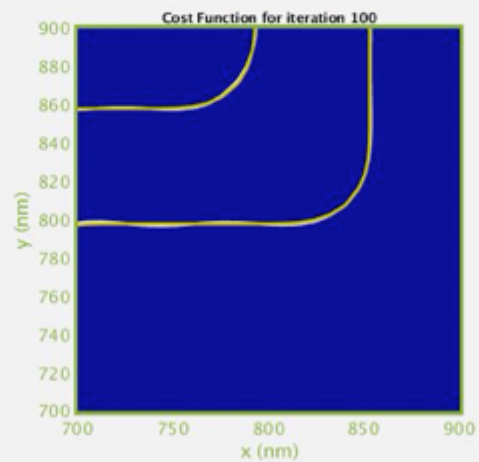
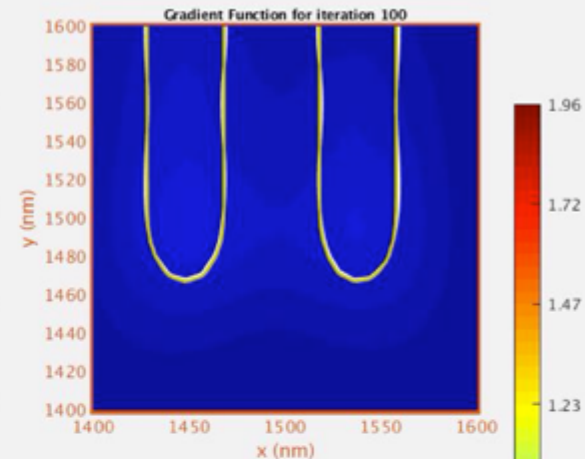
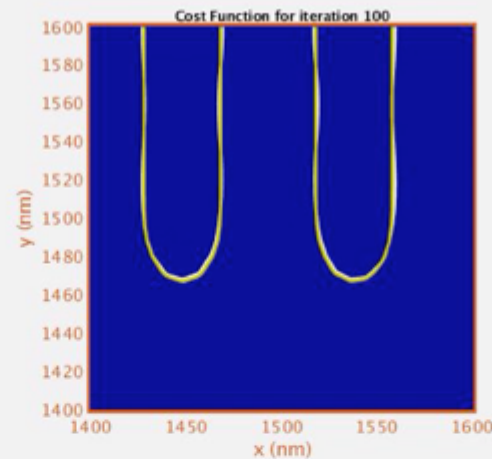
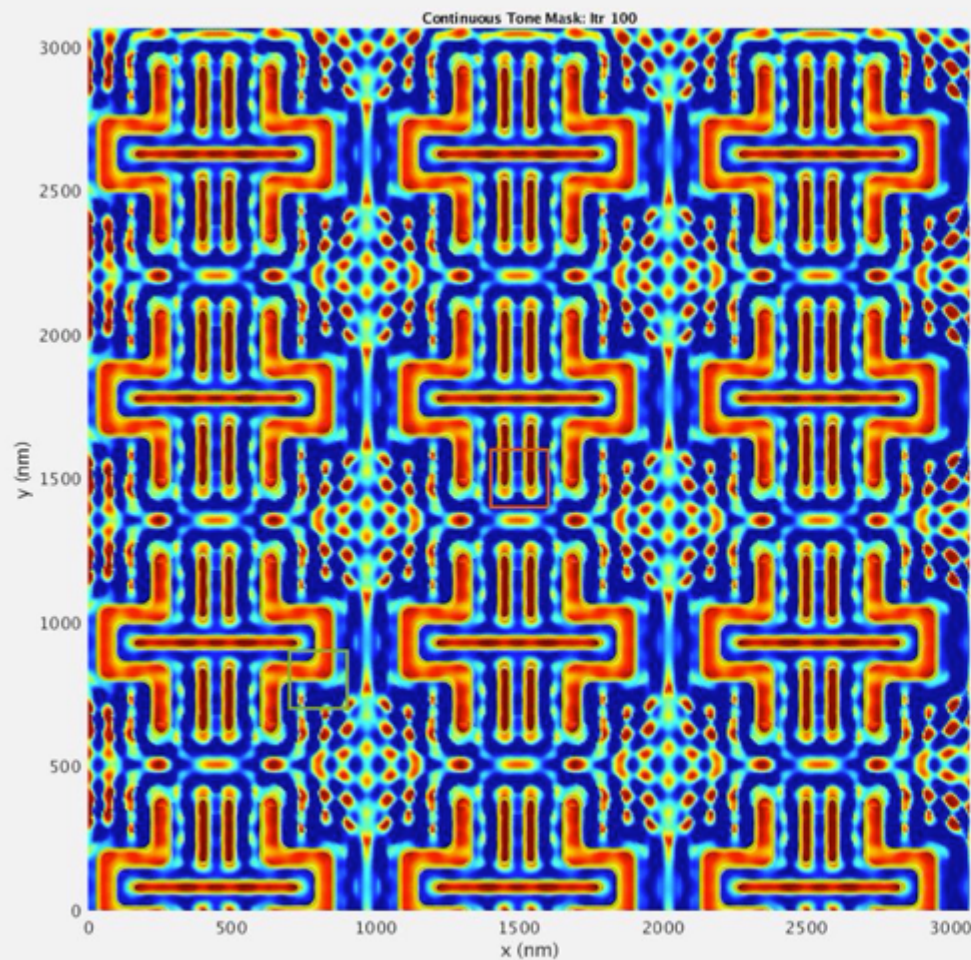


# TrueMask ILT Meets EPE Requirements

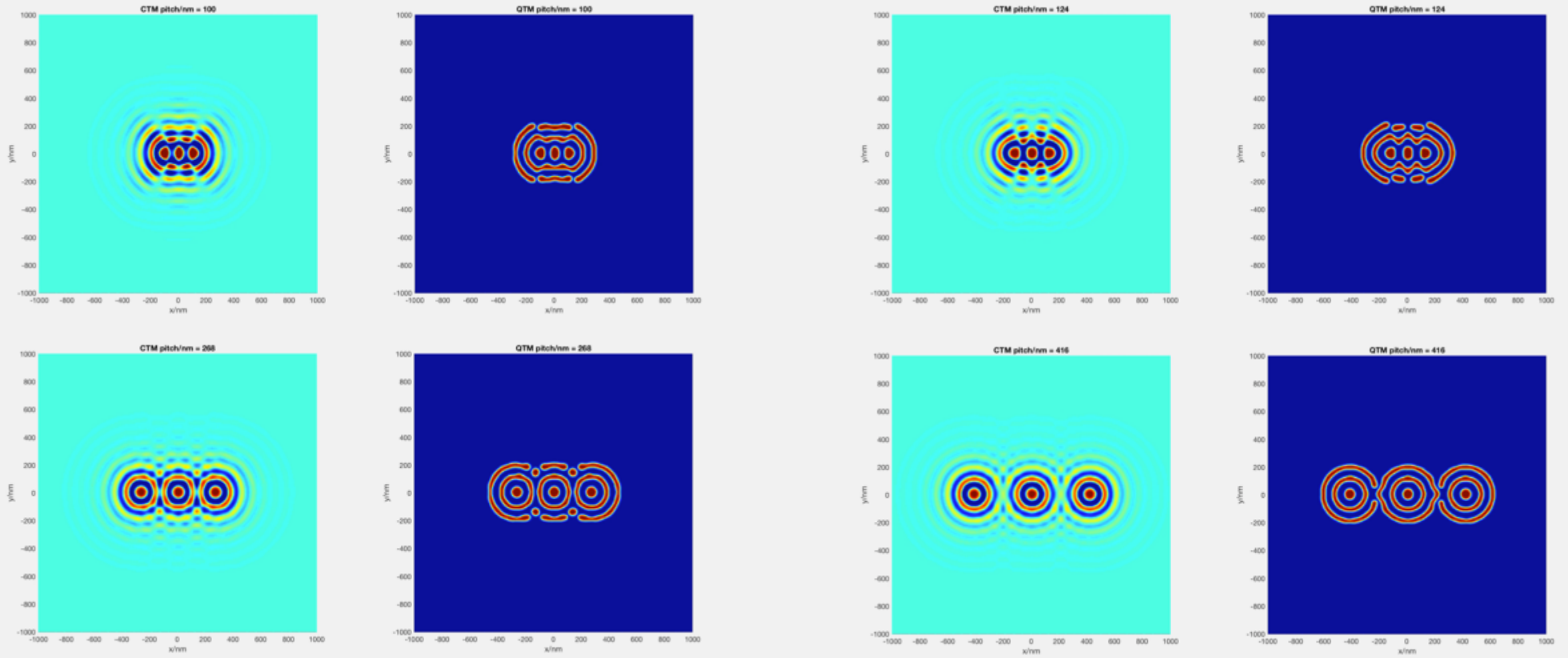




# TrueMask ILT Meets EPE Requirements



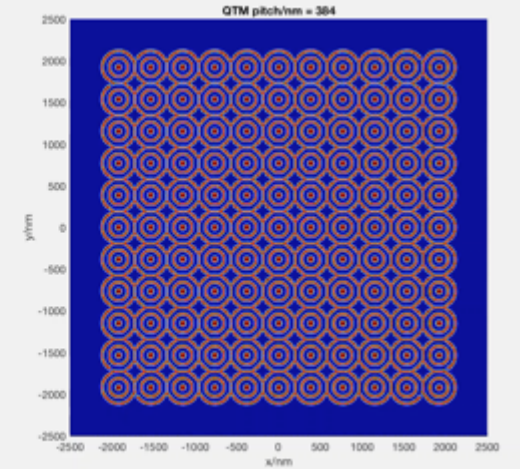
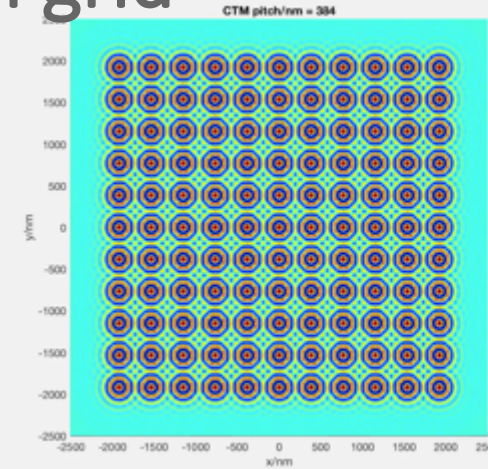
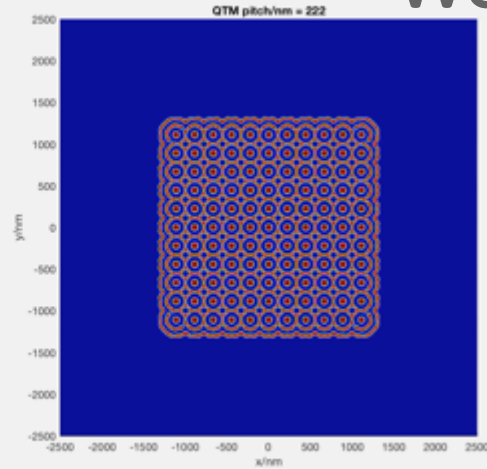
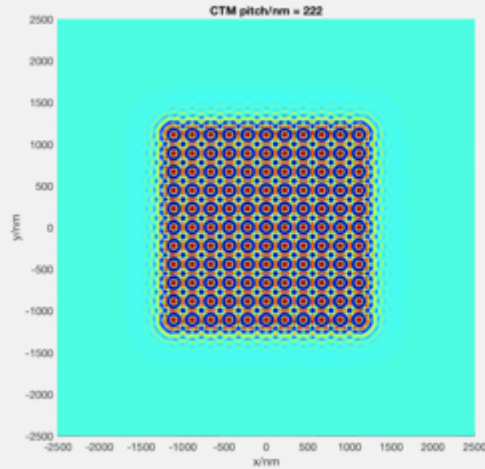
# TrueMask ILT Solutions are Continuous and Symmetric



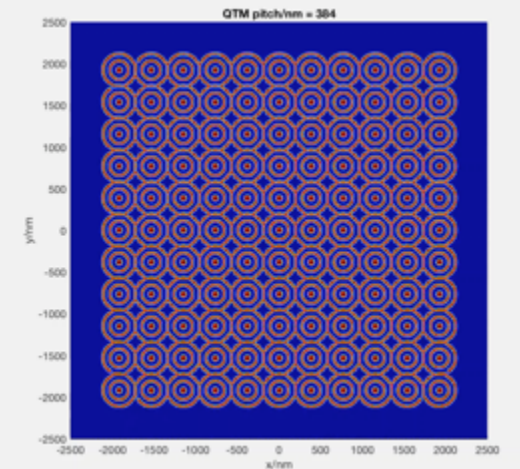
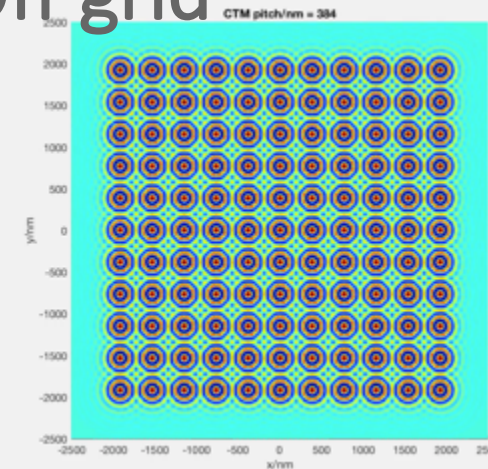
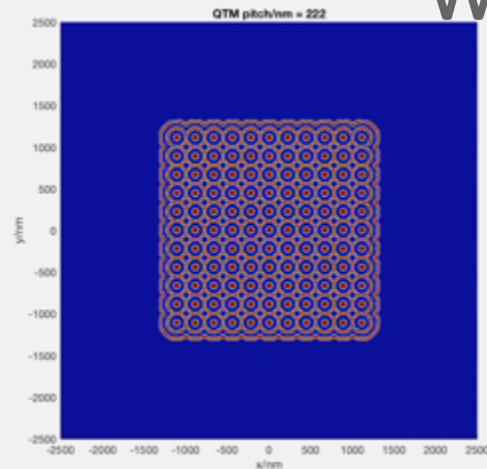
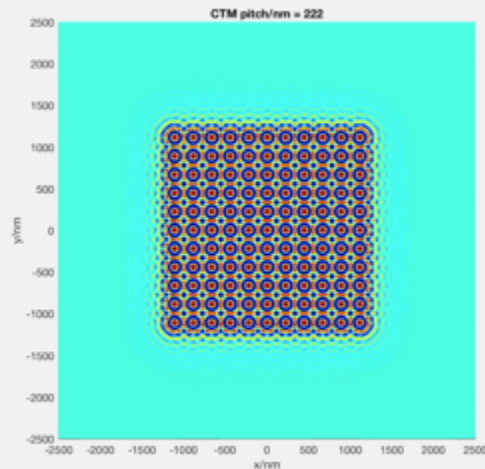


# TrueMask ILT Solutions are Continuous and Symmetric

## Works On grid

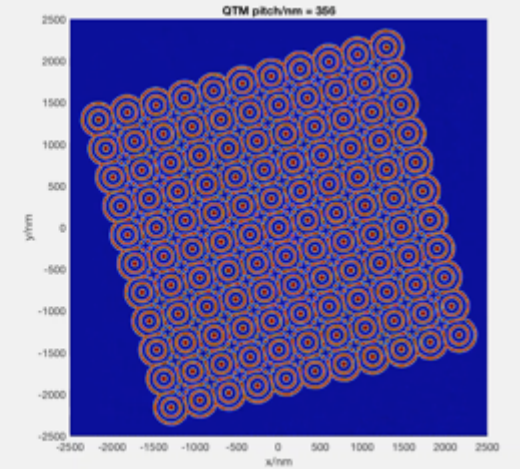
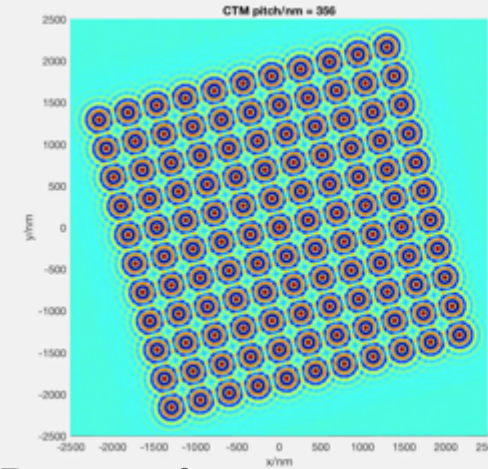
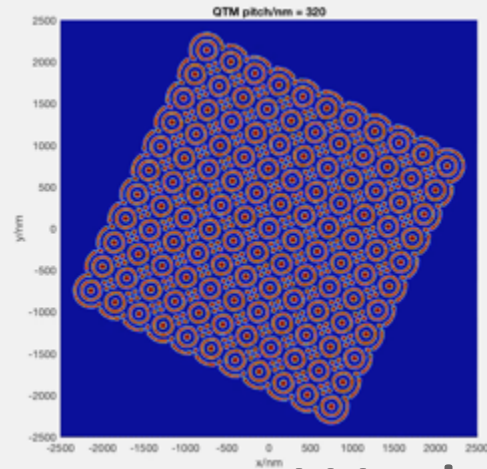
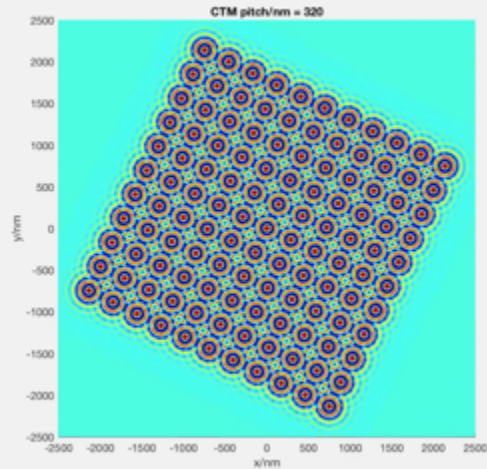
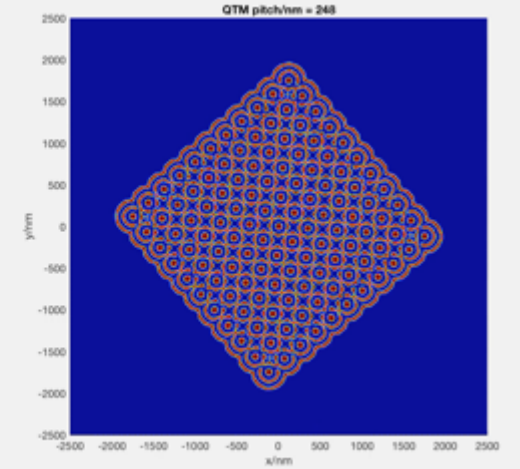
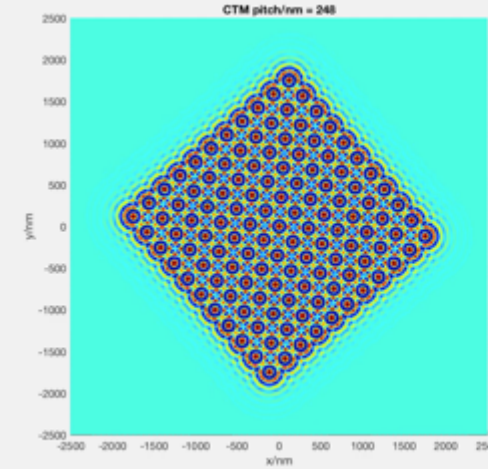
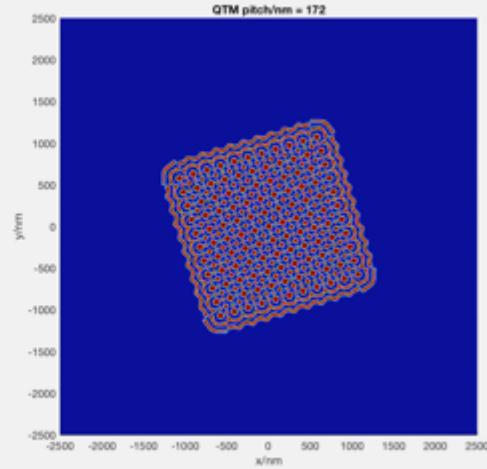
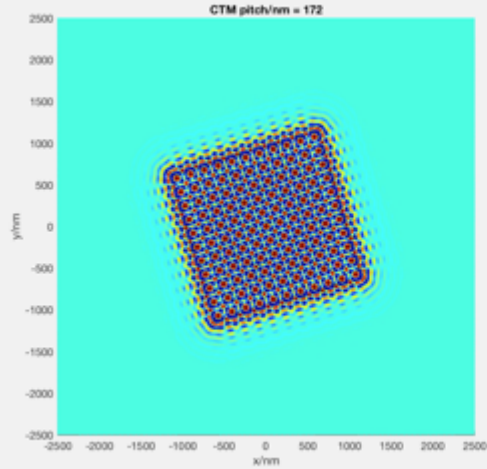


## Works Off grid





# TrueMask ILT Solutions are Continuous and Symmetric



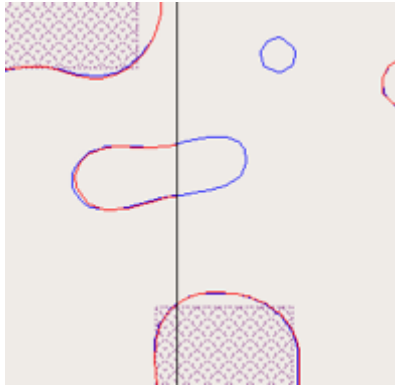
Works with Rotation



# The End Result: TrueMask ILT Does Full Chip in a Day and Meets All Manufacturing Requirements



**1-Day  
Run Time**



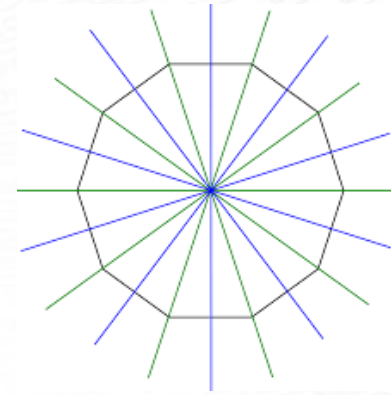
**No Stitching  
Errors**



**Resilient  
Masks**

**<0.1nm**

**EPE**



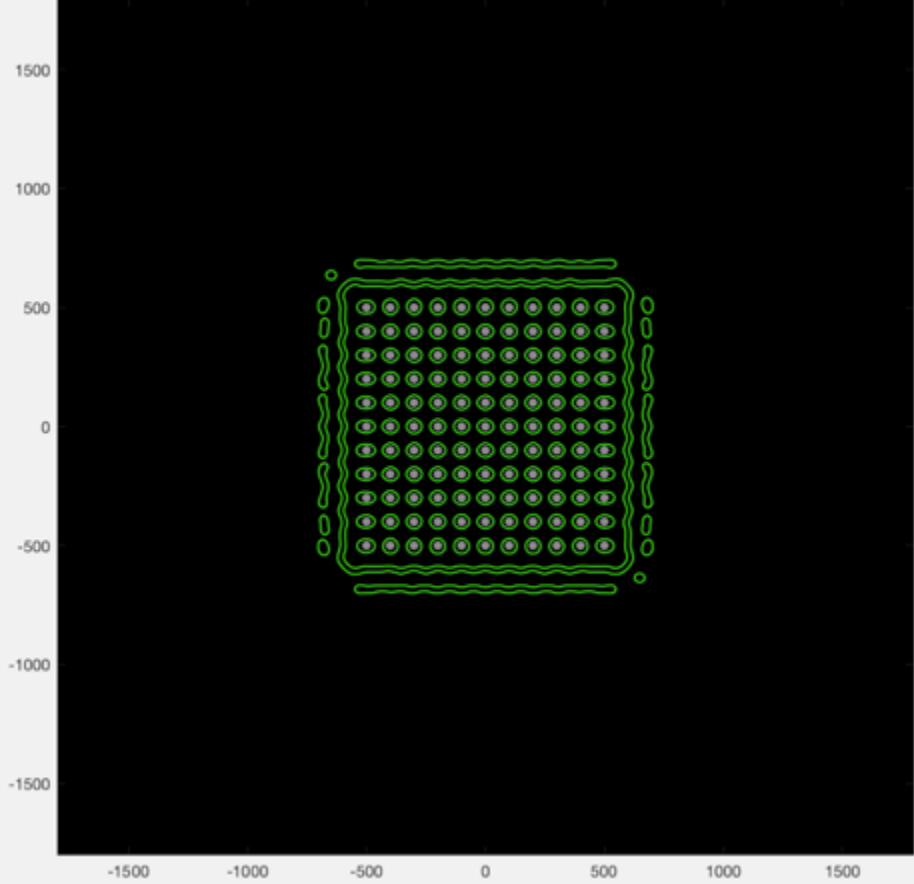
**Symmetry**



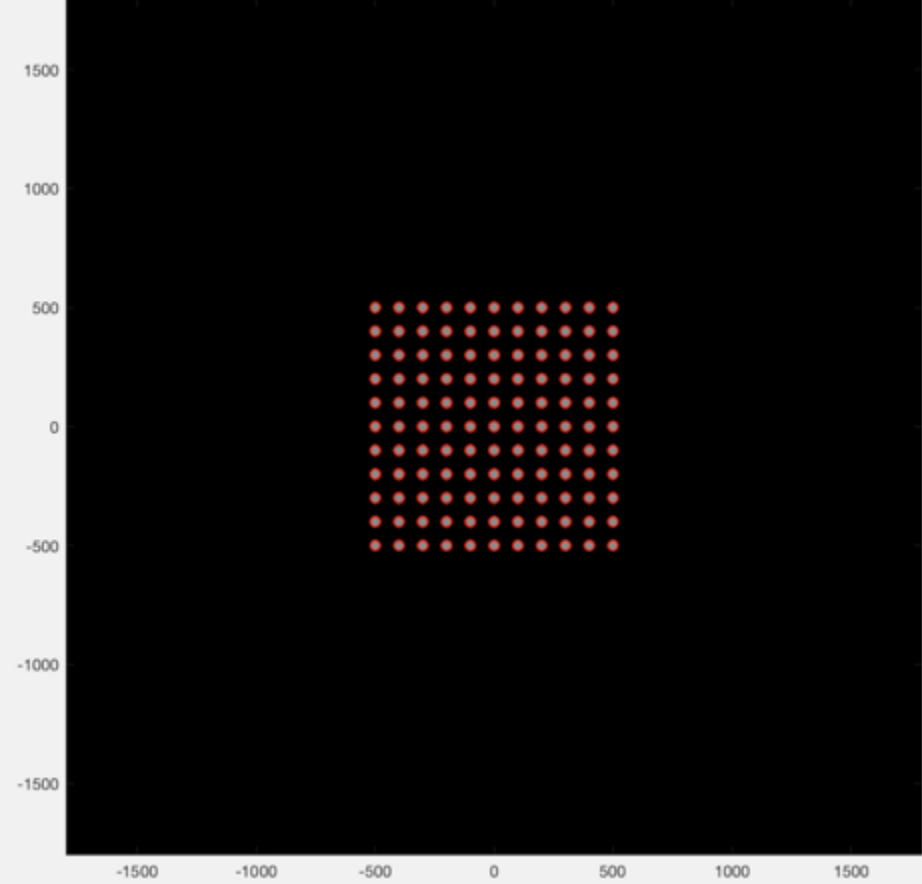
**MRC  
Clean**



# TrueMask ILT Results on Memory Design with Free-Form Source Demonstrated at Micron



TrueMask ILT curvilinear mask designs for different pitches & orientations

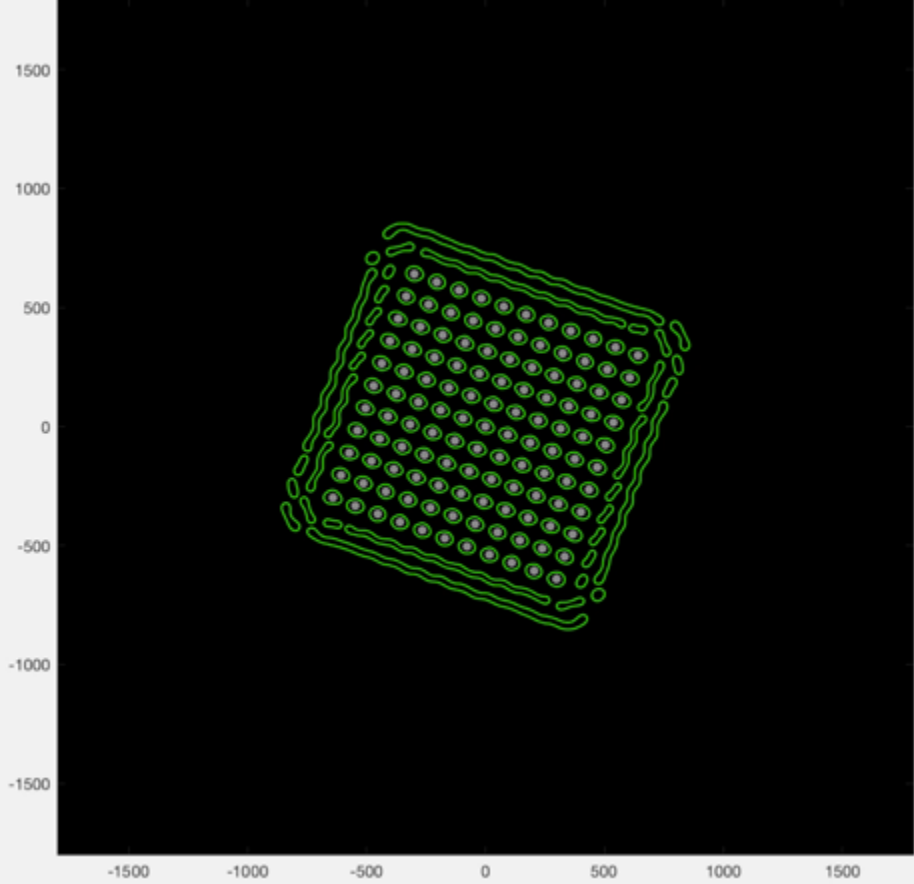


Corresponding wafer target & simulated wafer contours

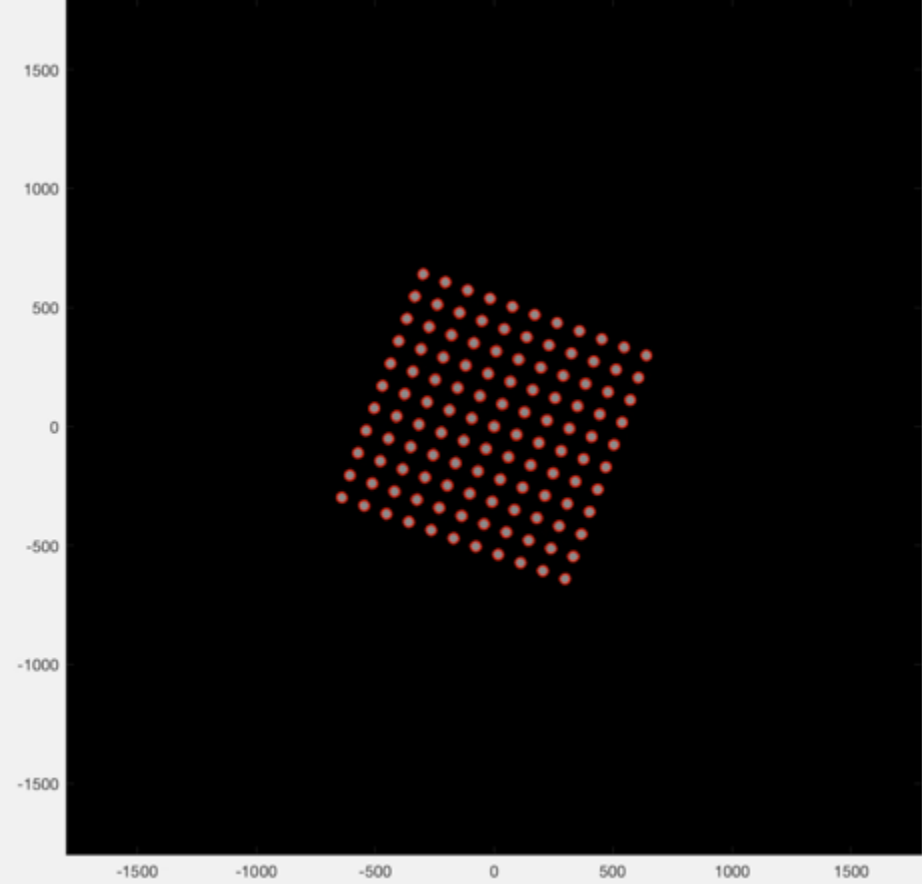




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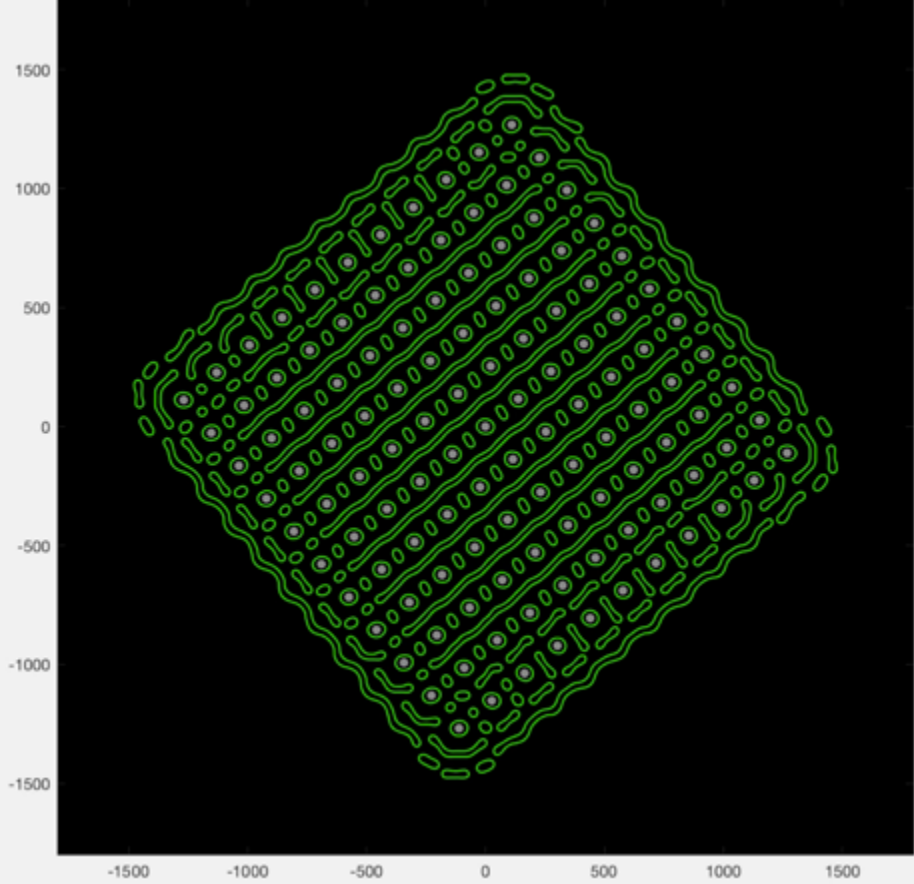
TrueMask ILT curvilinear mask designs for different pitches & orientations



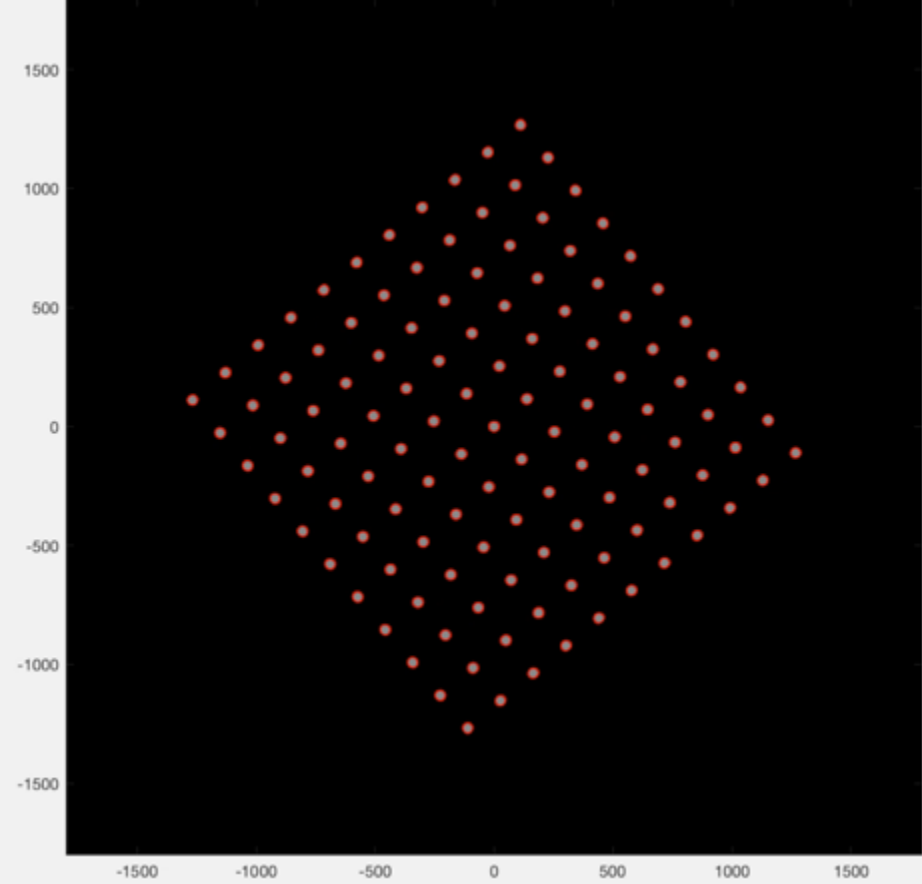
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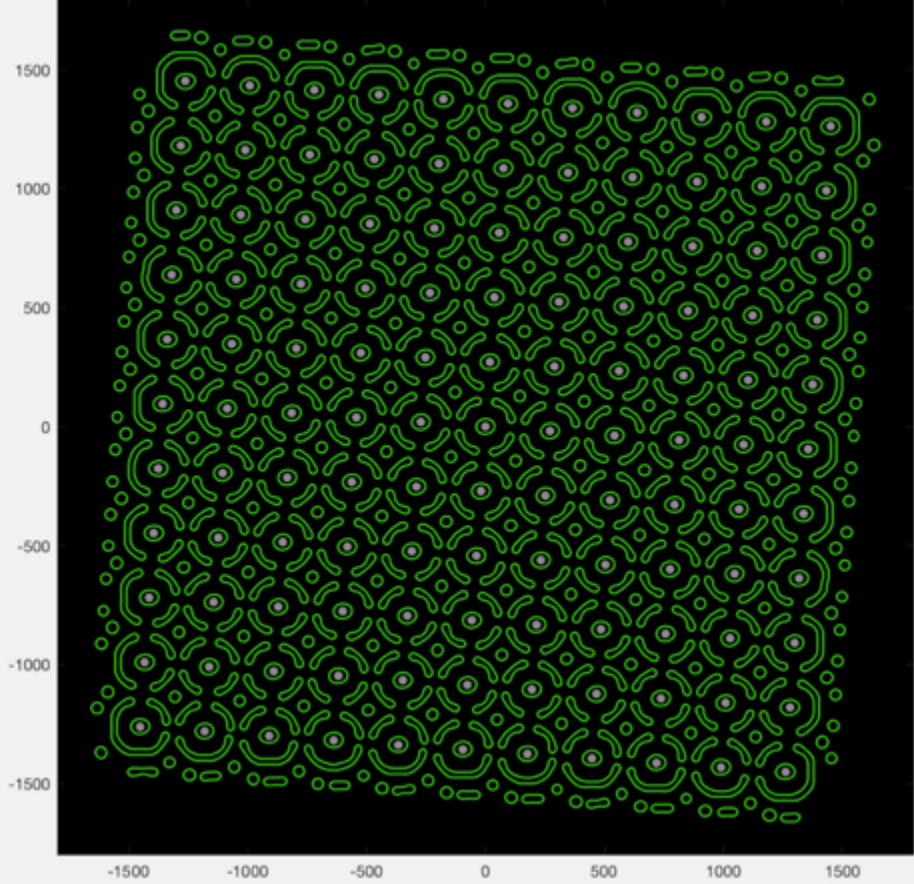
TrueMask ILT curvilinear mask designs for different pitches & orientations



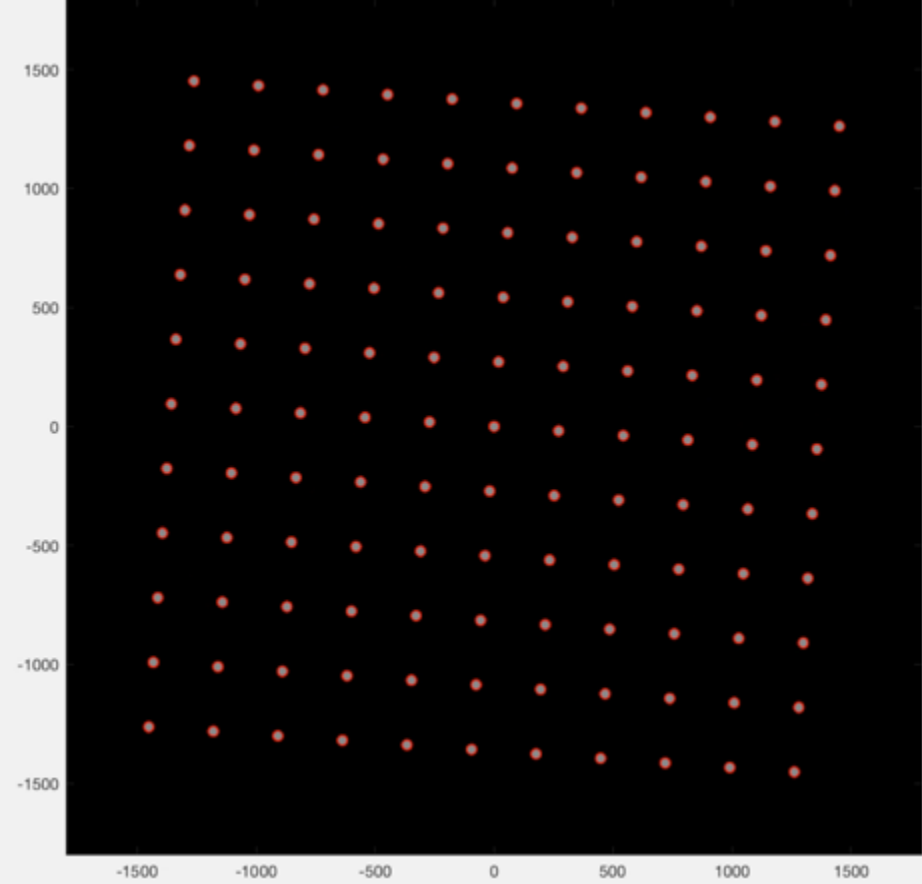
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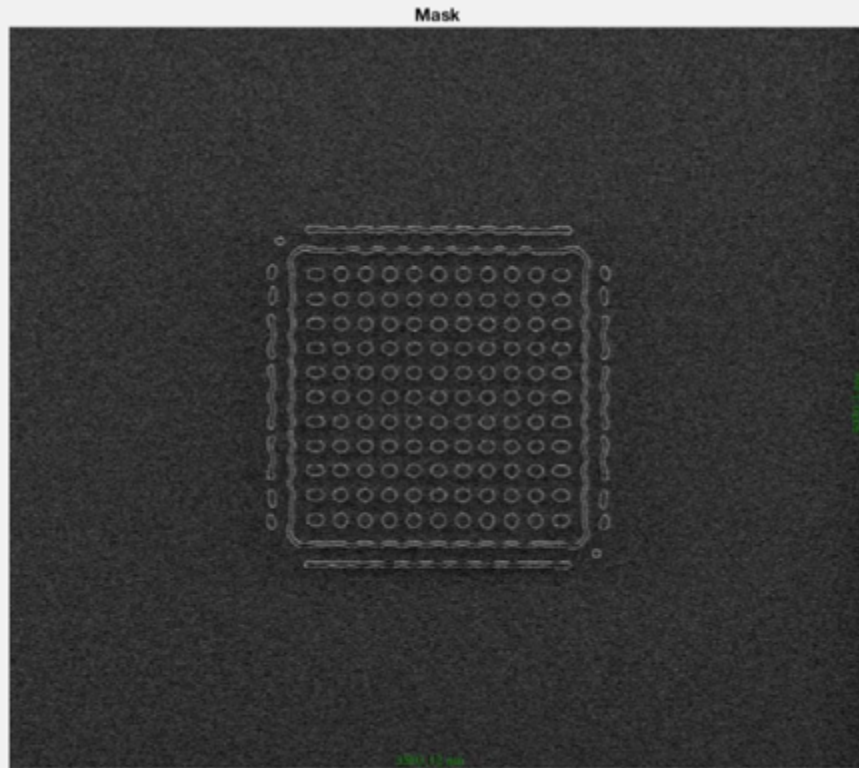


Corresponding wafer target & simulated wafer contours



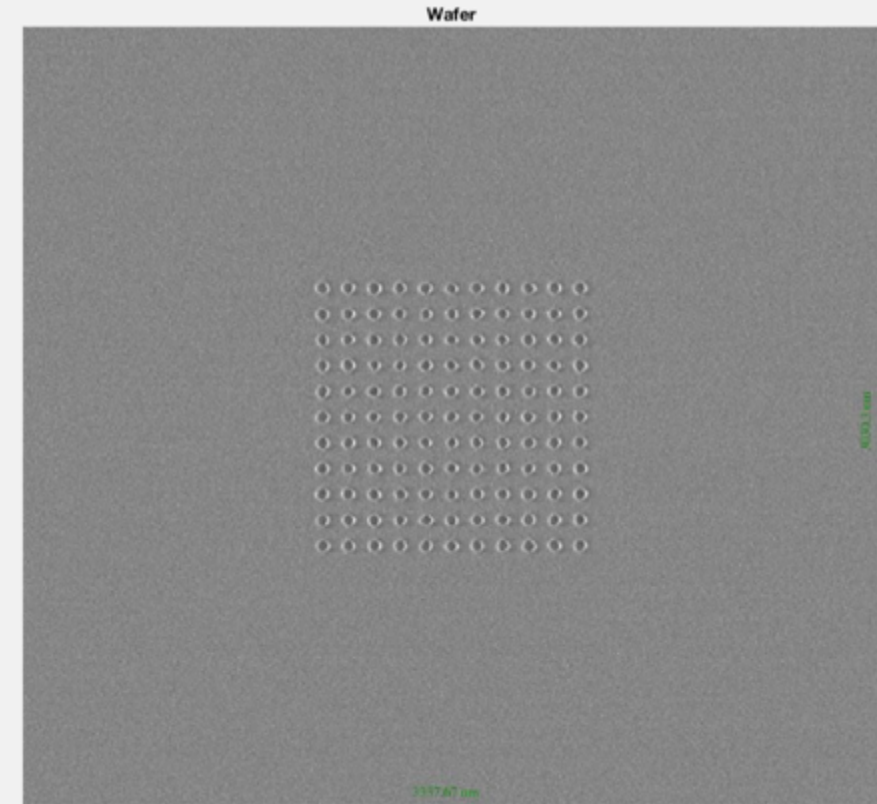


# Here is the Real Mask and Wafer Print!



TrueMask ILT curvilinear mask SEM  
for different pitches & orientations

Mask printed on NuFlare MBM-1000

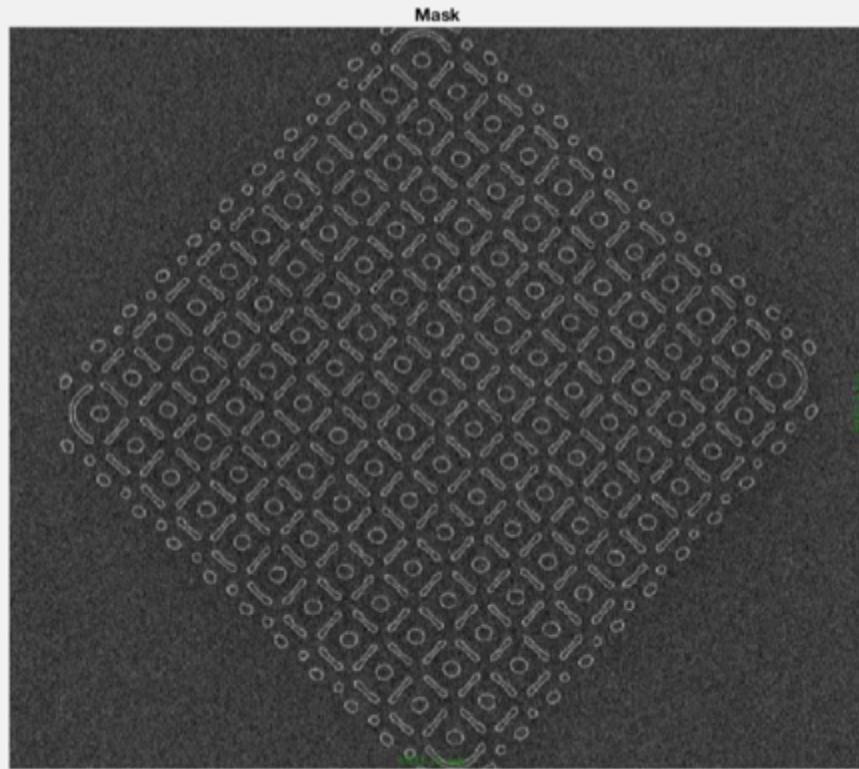


Corresponding wafer print SEM

Thanks to ASML for their help to acquire wafer  
images with eP5 platform

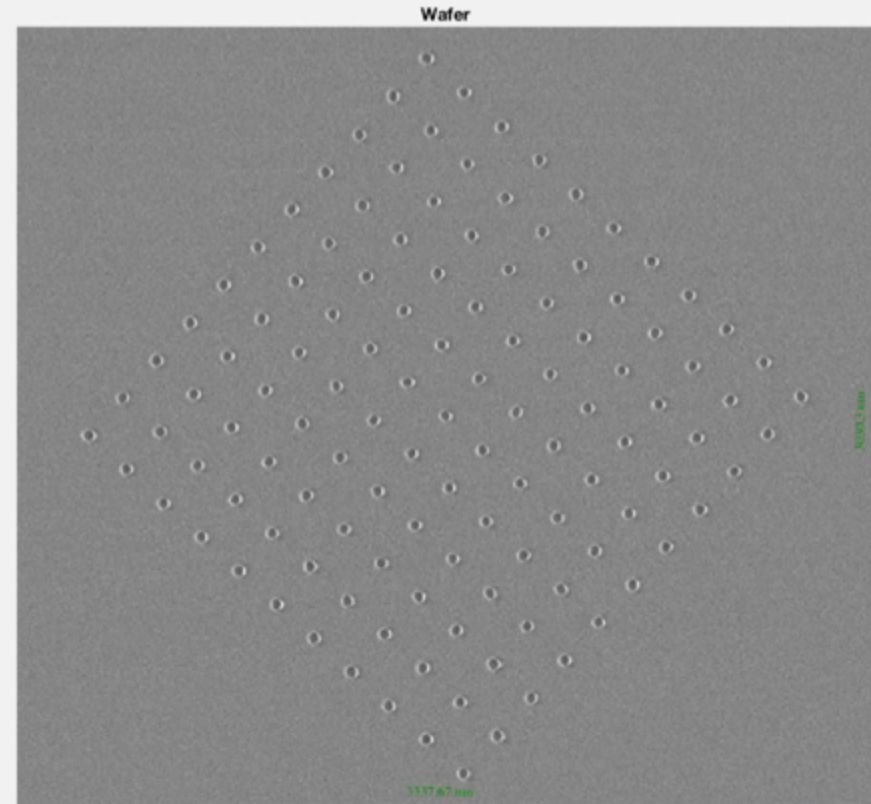


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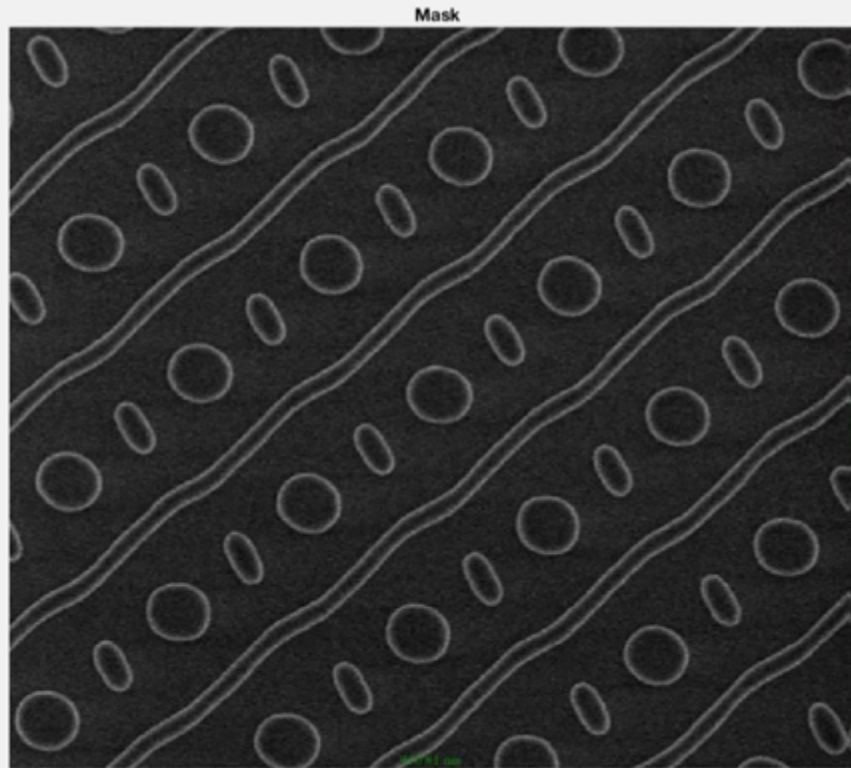


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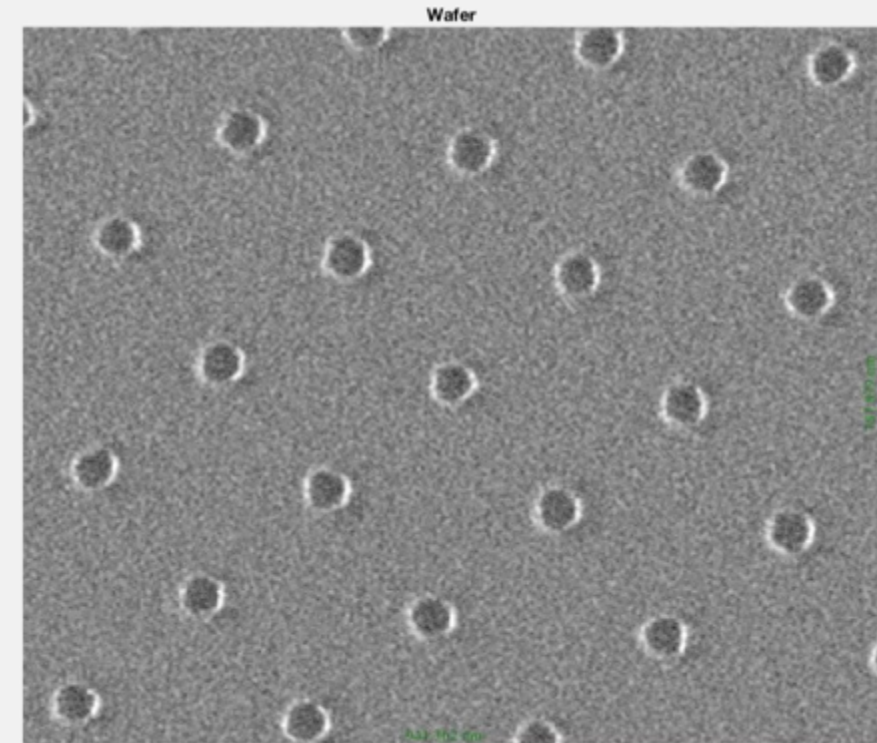


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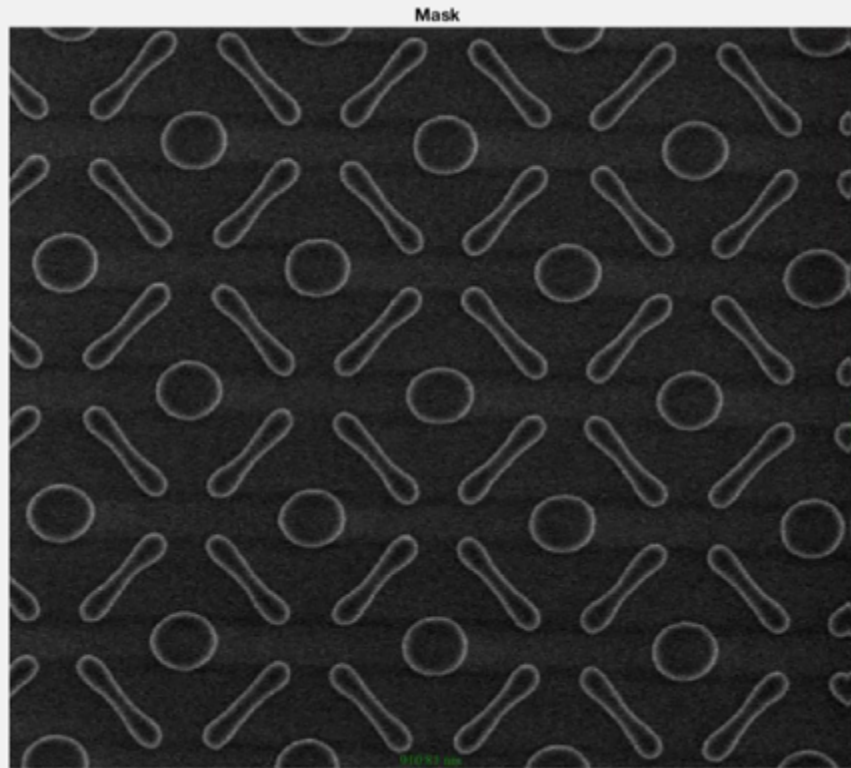
Corresponding wafer print SEM

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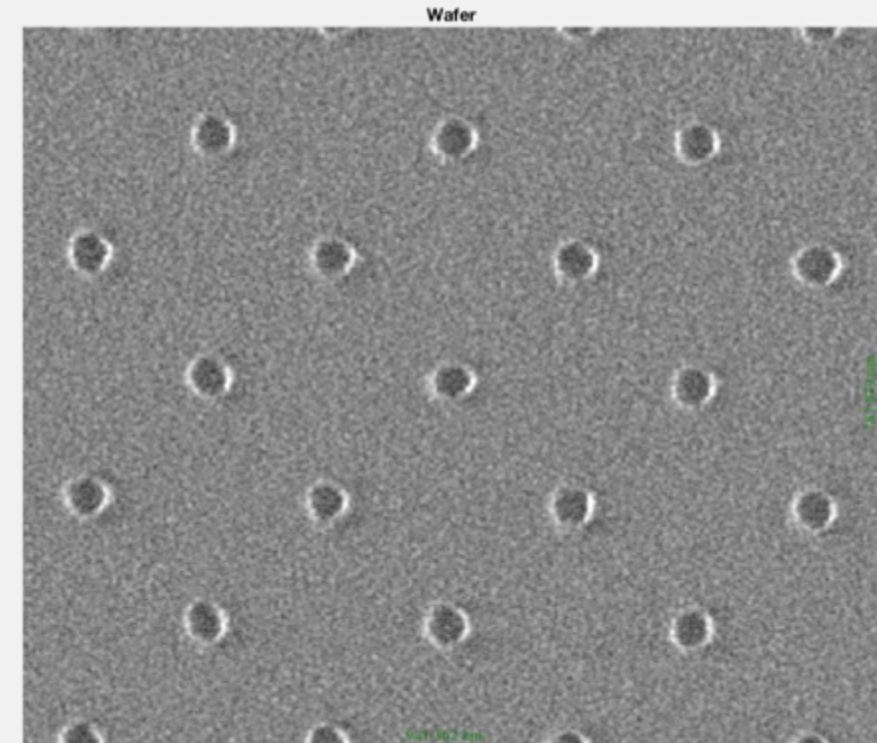


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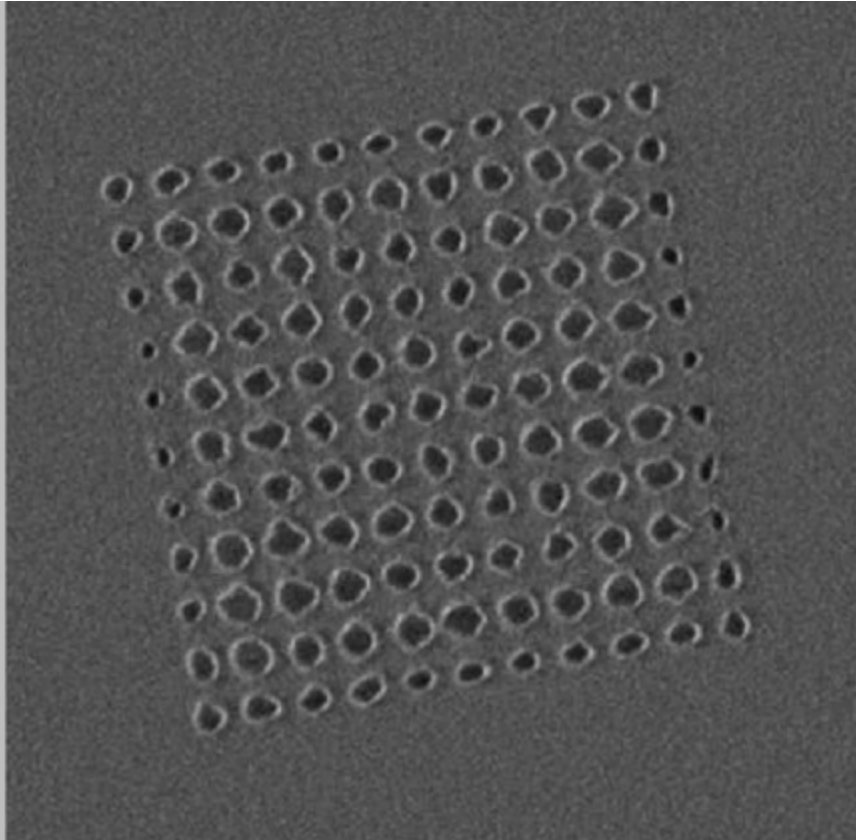


Corresponding wafer print SEM

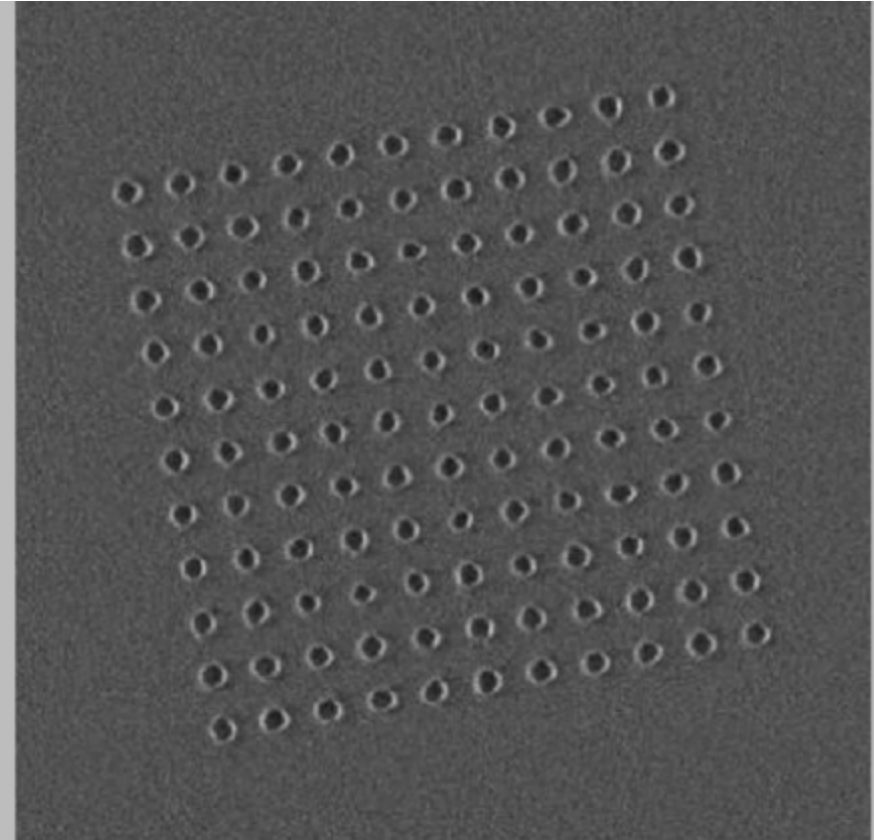
Thanks to ASML for their help to acquire wafer  
images with eP5 platform



# Wafer Results Show TrueMask ILT Produces Much Larger Process Windows than OPC



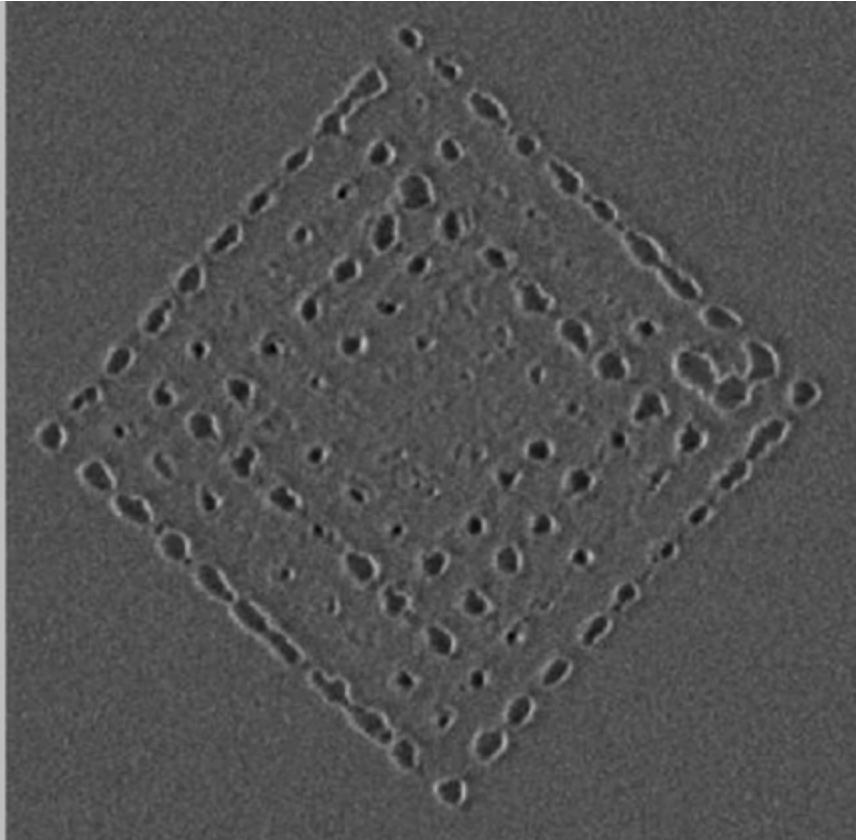
OPC Wafer Print at Different  
Process Conditions



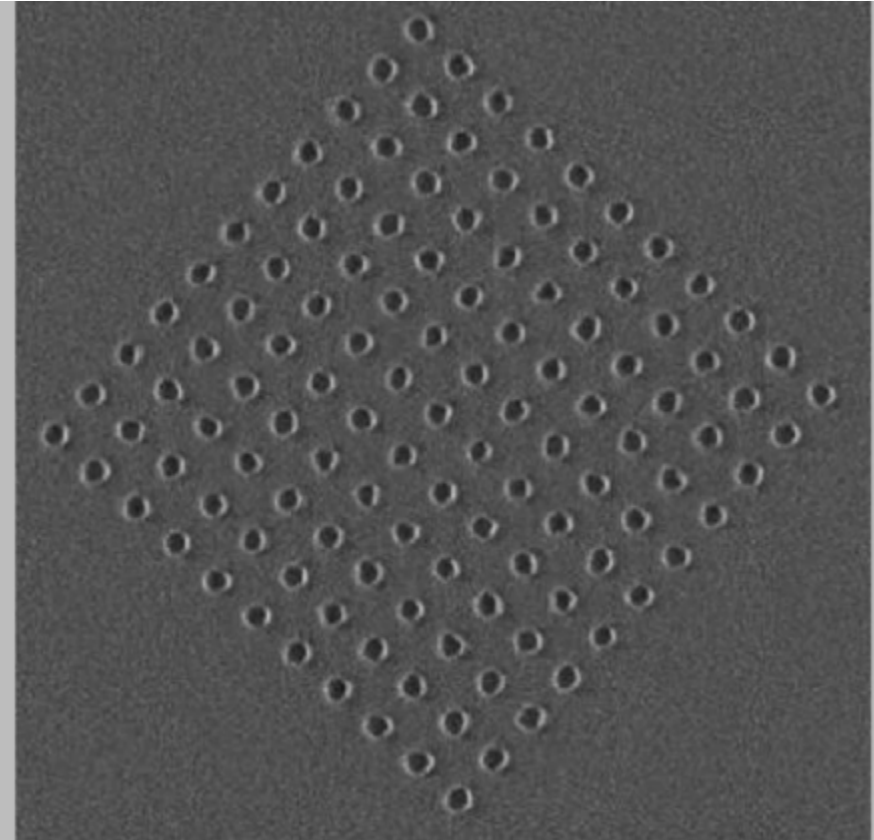
TrueMask ILT Wafer Print for the  
Same Process Conditions



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OPC Wafer Print at Different  
Process Conditions

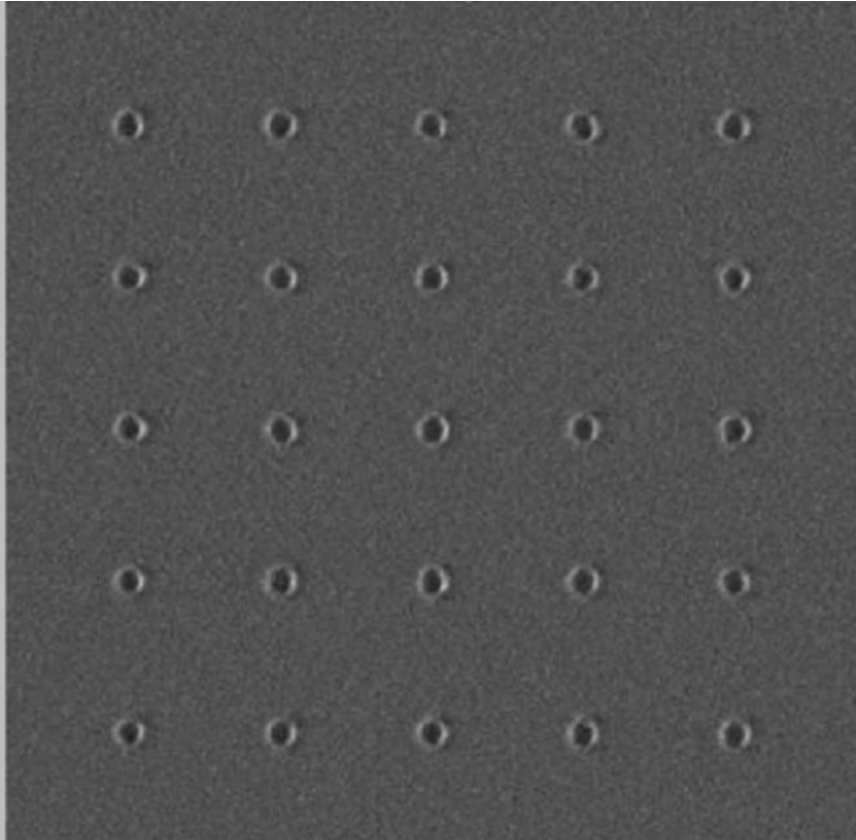


TrueMask ILT Wafer Print for the  
Same Process Conditions

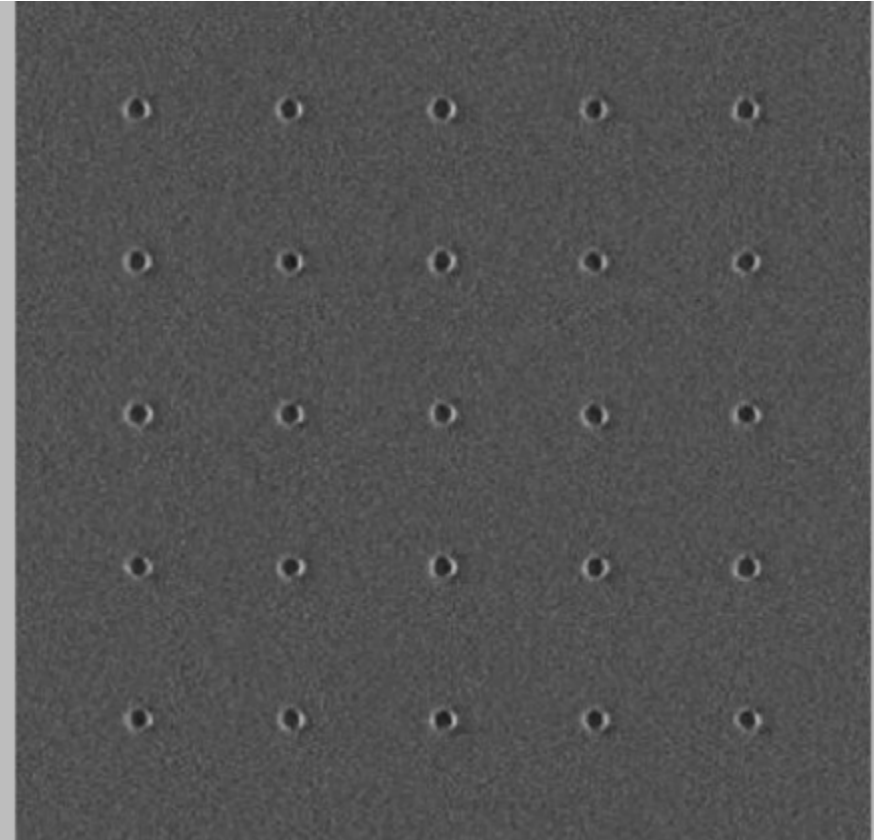




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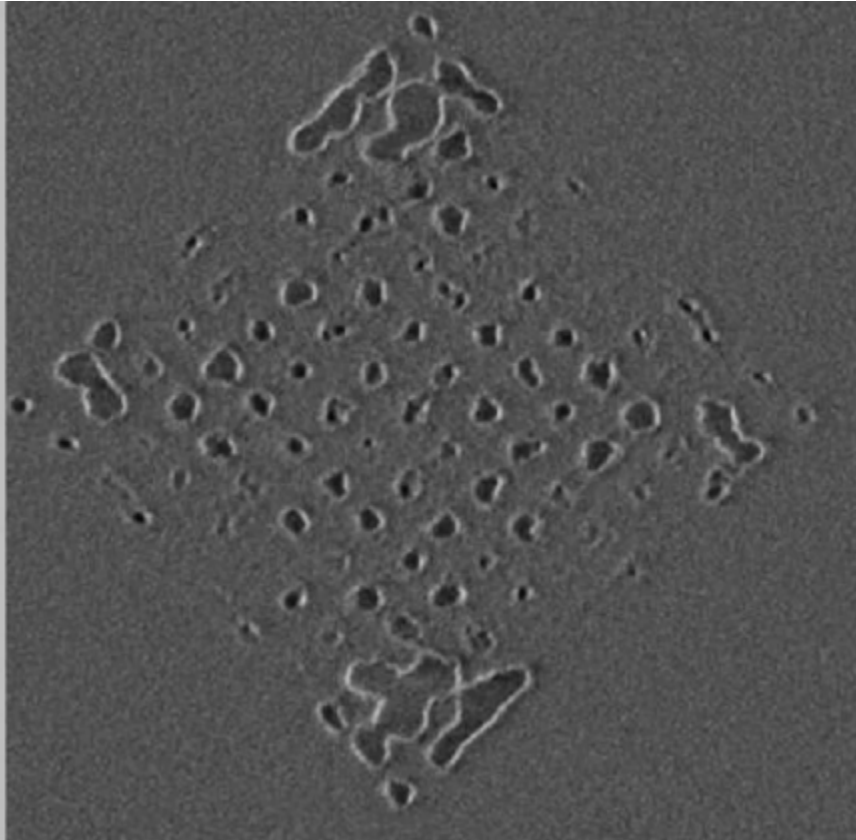
OPC Wafer Print at Different  
Process Conditions



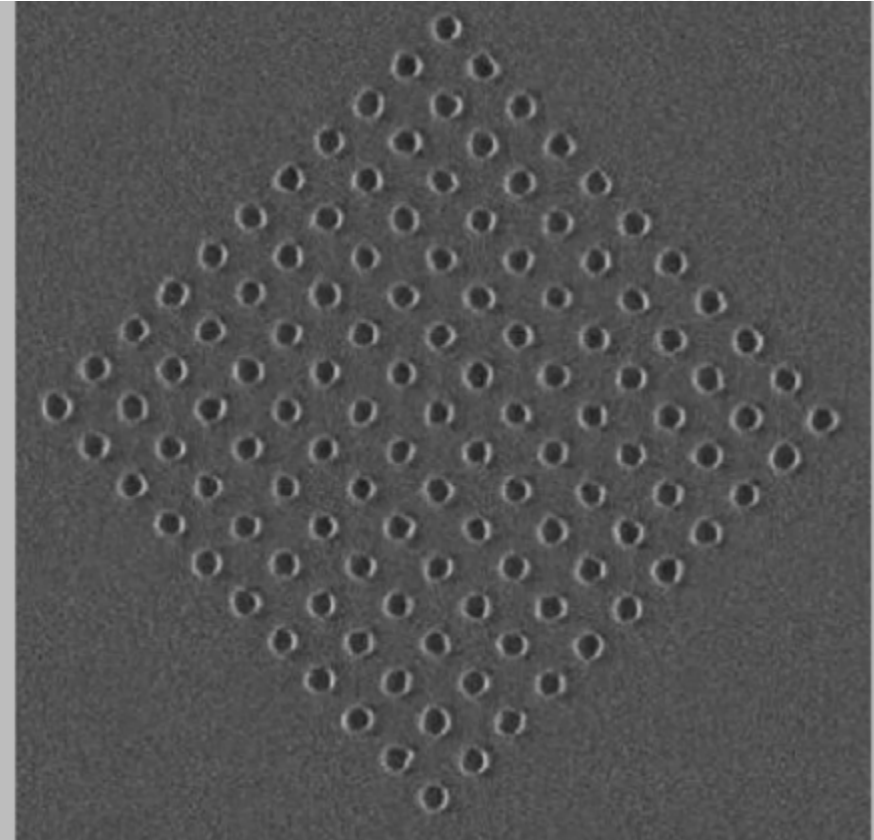
TrueMask ILT Wafer Print for the  
Same Process Conditions



# Wafer Results Show TrueMask ILT Produces Much Larger Process Windows than OPC



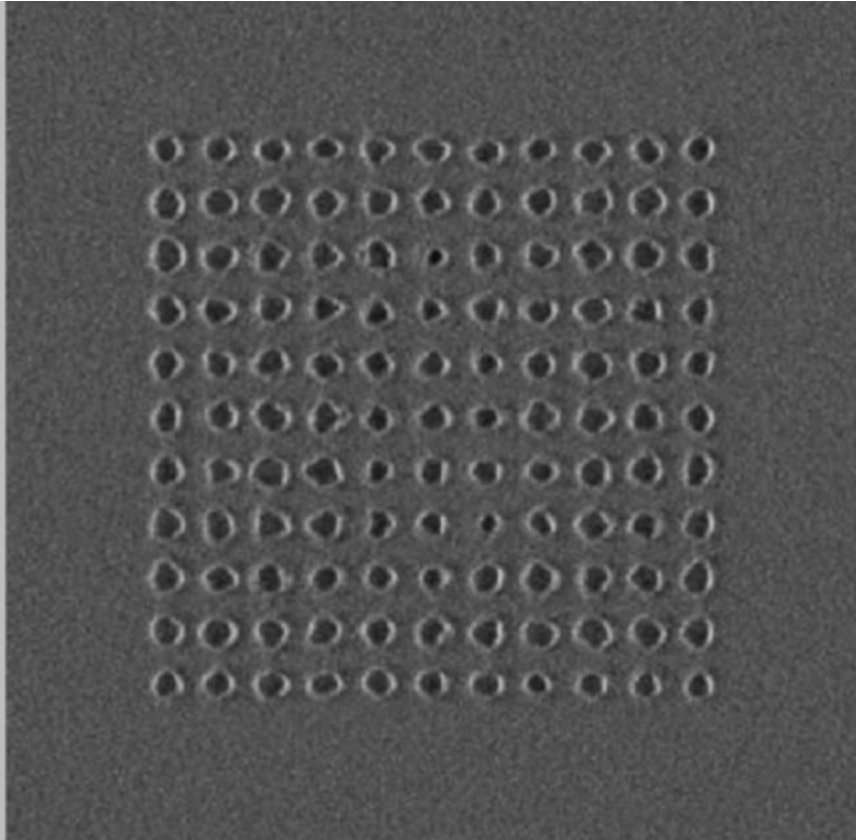
OPC Wafer Print at Different  
Process Conditions



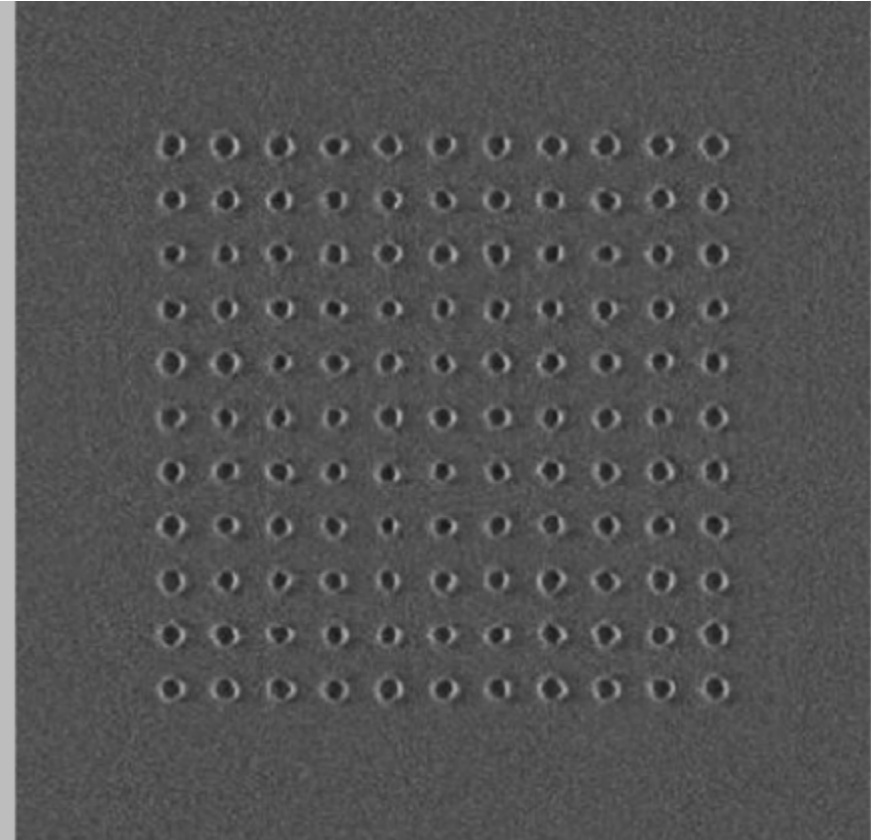
TrueMask ILT Wafer Print for the  
Same Process Conditions



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OPC Wafer Print at Different  
Process Conditions

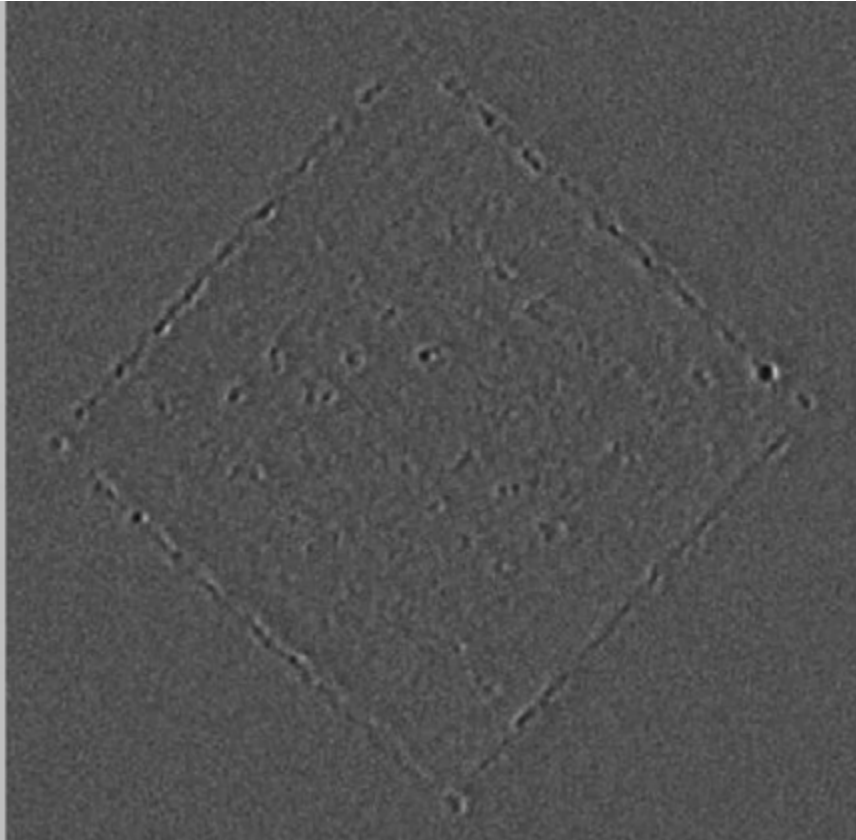


TrueMask ILT Wafer Print for the  
Same Process Conditions

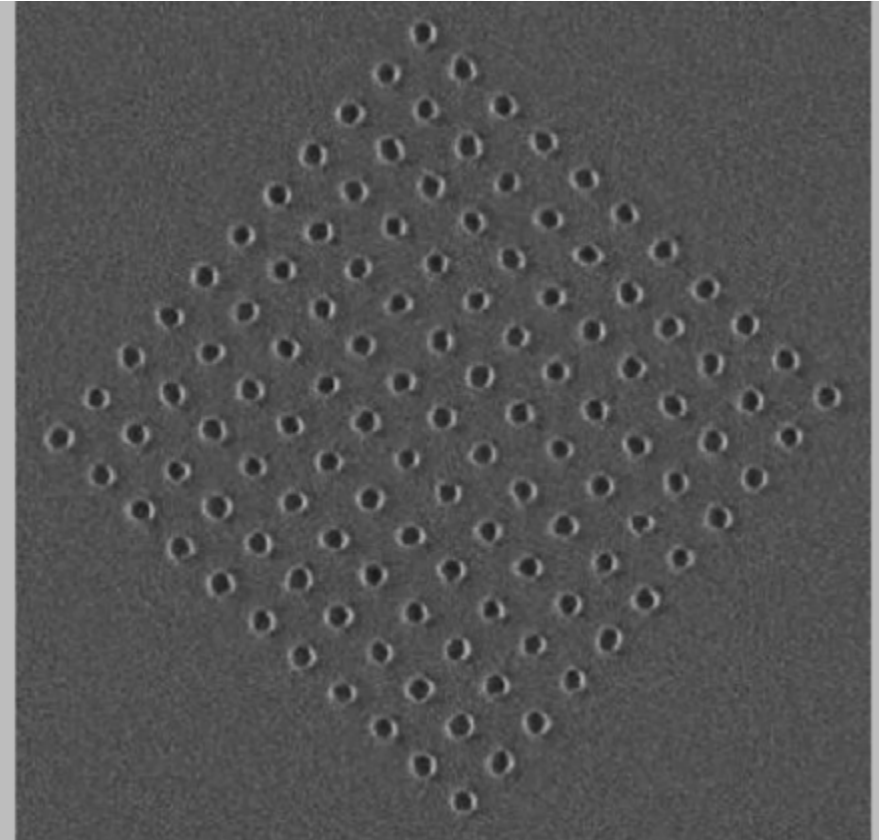




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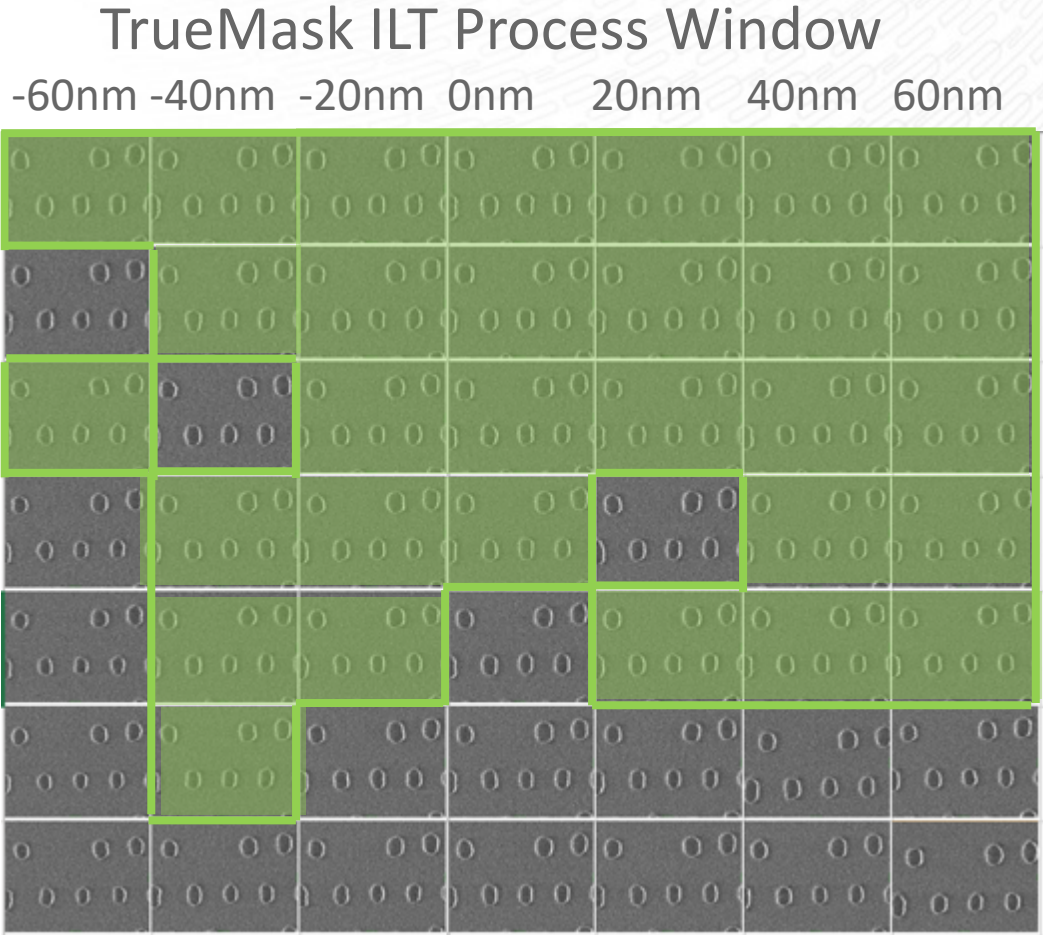
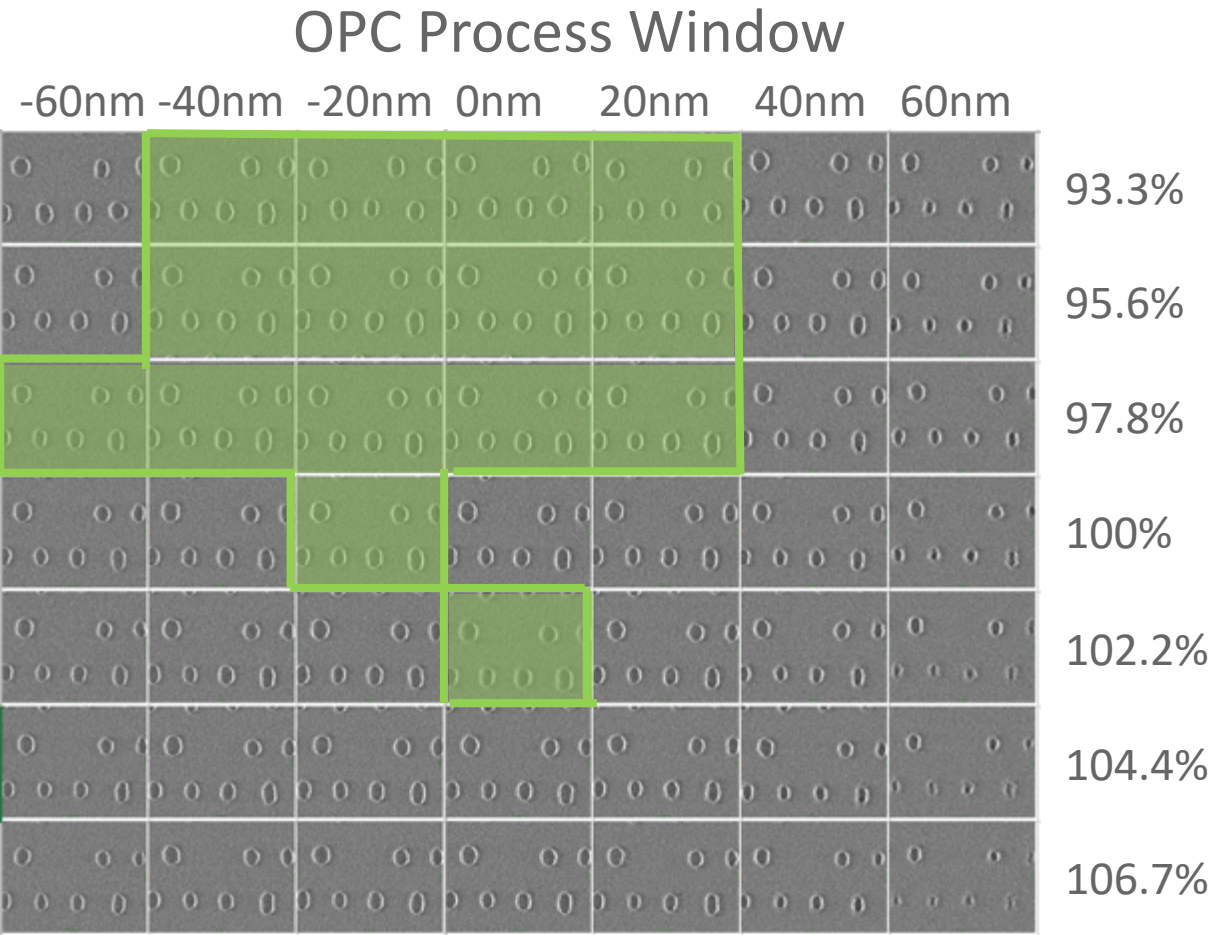
OPC Wafer Print at Different  
Process Conditions



TrueMask ILT Wafer Print for the  
Same Process Conditions



# Wafer Results Show TrueMask ILT Produces Much Larger Process Windows than OPC



62.8nm Random Contact



Green: <10% CD Variation



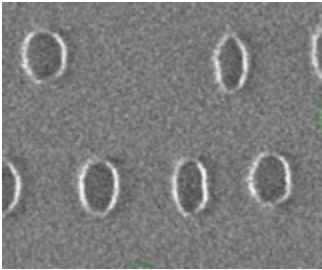
# Wafer Results Show TrueMask ILT Produces Much Larger Process Windows than OPC

OPC Process Window

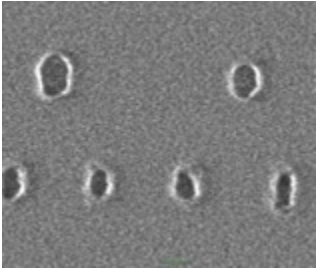
|          | Dose<br>(mJ) | Defocus (nm) |      |      |      |      |      |      | Dose(%) |
|----------|--------------|--------------|------|------|------|------|------|------|---------|
|          |              | -60          | -40  | -20  | 0    | 20   | 40   | 60   |         |
| Latitude | 21           | 55.4         | 59.6 | 62.5 | 61.2 | 60.5 | 51.6 | 41.8 | 93.3%   |
|          | 21.5         | 56.3         | 57.3 | 63.7 | 61.0 | 58.1 | 52.9 | 40.3 | 95.6%   |
|          | 22           | 57.3         | 60.8 | 61.0 | 60.8 | 57.1 | 48.3 | 41.6 | 97.8%   |
|          | 22.5         | 54.0         | 52.8 | 60.1 | 55.8 | 54.7 | 52.1 | 39.3 | 100.0%  |
|          | 23           | 49.4         | 54.4 | 55.3 | 60.3 | 54.5 | 49.2 | 36.1 | 102.2%  |
|          | 23.5         | 49.2         | 50.9 | 54.5 | 55.0 | 51.6 | 46.1 | 33.9 | 104.4%  |
|          | 24           | 54.0         | 56.2 | 54.8 | 49.9 | 50.9 | 44.7 | 28.6 | 106.7%  |

TrueMask ILT Process Window

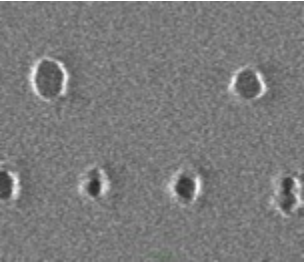
|          | Dose<br>(mJ) | Defocus (nm) |      |      |      |      |      |      | Dose(%) |
|----------|--------------|--------------|------|------|------|------|------|------|---------|
|          |              | -60          | -40  | -20  | 0    | 20   | 40   | 60   |         |
| Latitude | 21           | 57.7         | 60.5 | 59.6 | 64.1 | 58.8 | 62.1 | 58.4 | 93.3%   |
|          | 21.5         | 54.0         | 56.9 | 58.1 | 60.9 | 59.0 | 62.8 | 59.4 | 95.6%   |
|          | 22           | 60.6         | 55.4 | 59.3 | 60.3 | 57.9 | 59.5 | 58.8 | 97.8%   |
|          | 22.5         | 54.5         | 57.7 | 57.6 | 60.6 | 56.2 | 59.4 | 57.9 | 100.0%  |
|          | 23           | 52.0         | 56.5 | 57.0 | 56.2 | 57.3 | 60.9 | 58.3 | 102.2%  |
|          | 23.5         | 52.2         | 56.7 | 55.1 | 54.6 | 54.9 | 55.6 | 54.7 | 104.4%  |
|          | 24           | 48.6         | 52.7 | 51.6 | 50.8 | 56.1 | 52.3 | 56.1 | 106.7%  |



Best Focus  
Norm Dose

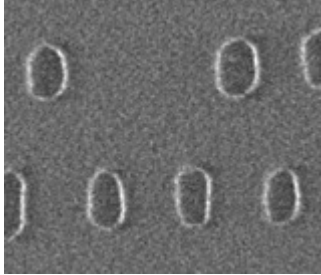


60nm Defocus  
Norm Dose

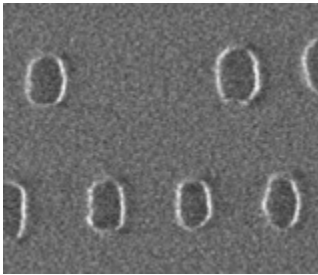


60nm Defocus  
93.33% Dose

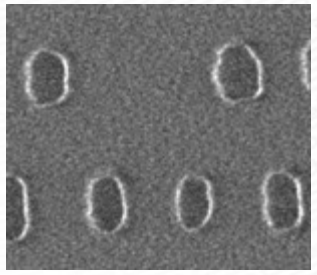
62.8nm Random Contact



Best Focus  
Norm Dose



60nm Defocus  
Norm Dose



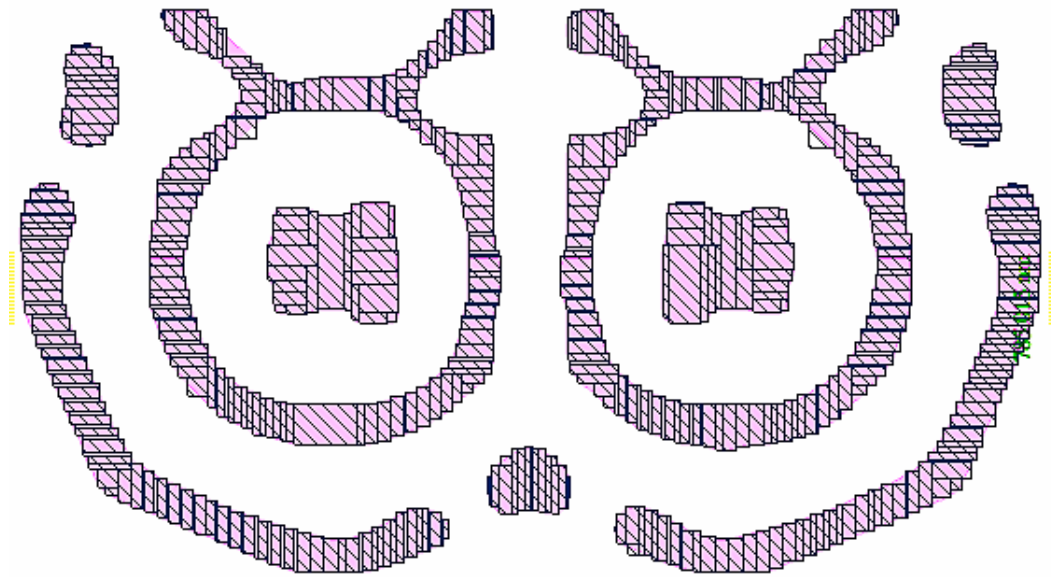
60nm Defocus  
93.33% Dose

Green: <10% CD Variation

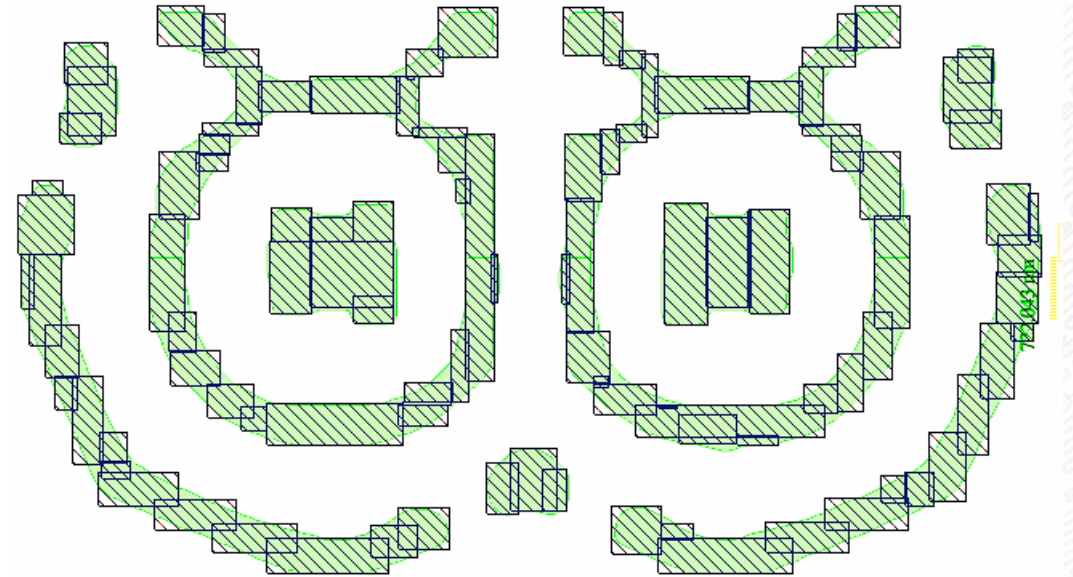




# Is Curvilinear ILT for VSB Mask Writers Hopeless? Or Can Overlapping Shots & Simulation Save the Day?



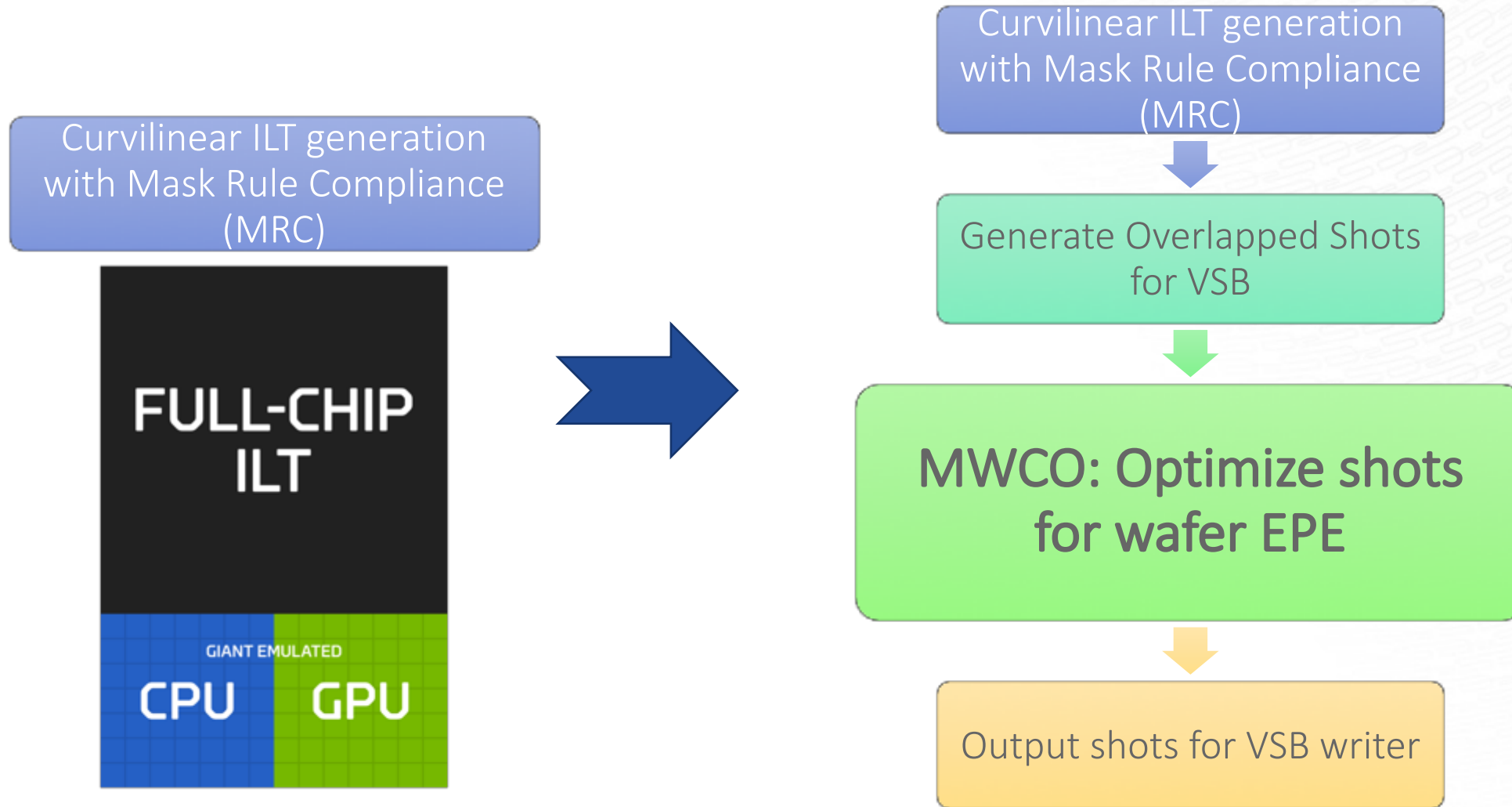
VSB Conventional Shots  
557 Shots



VSB Overlapping Shots  
103 Shots

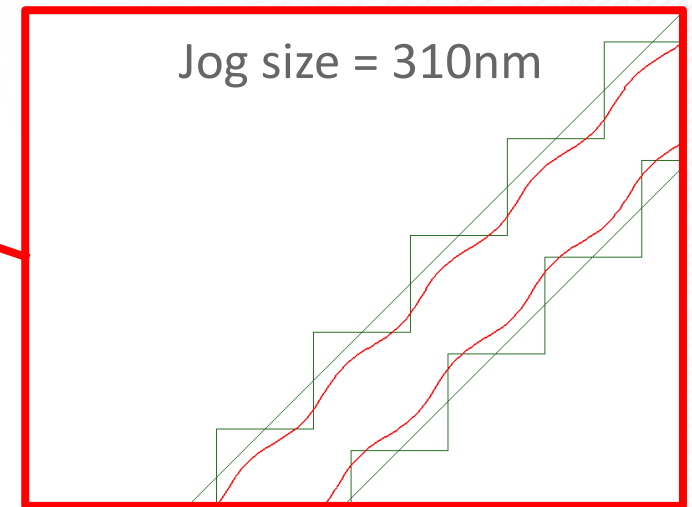
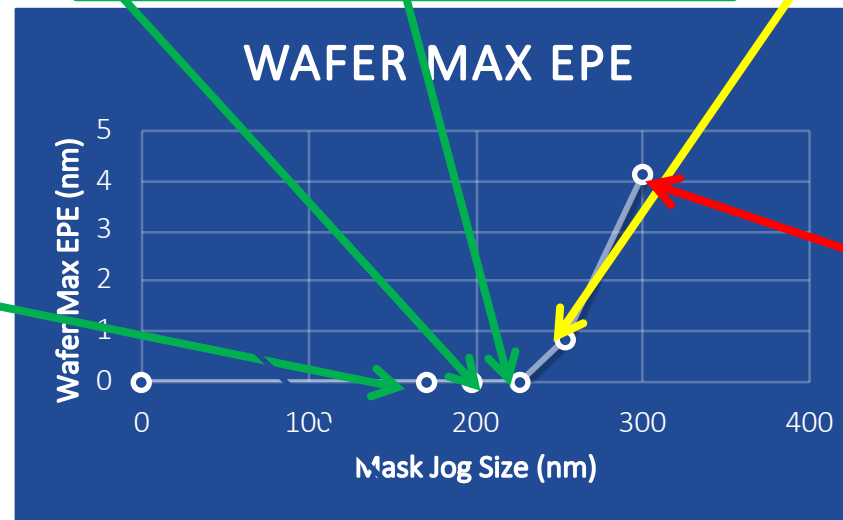
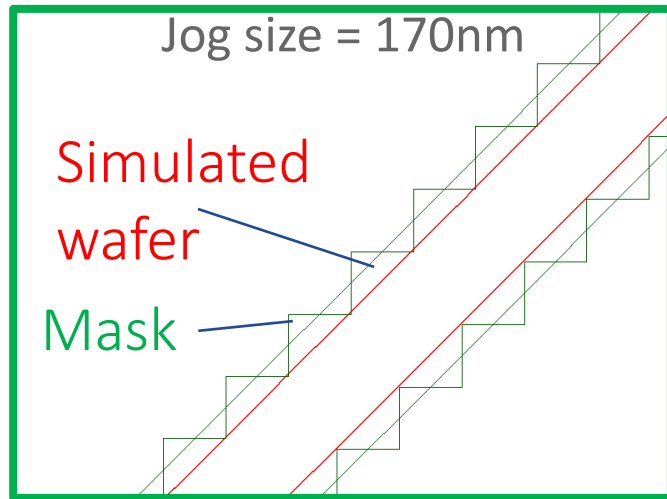
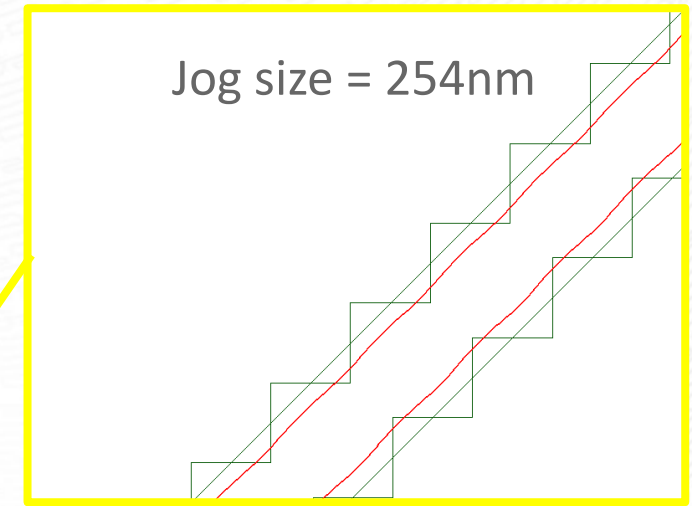
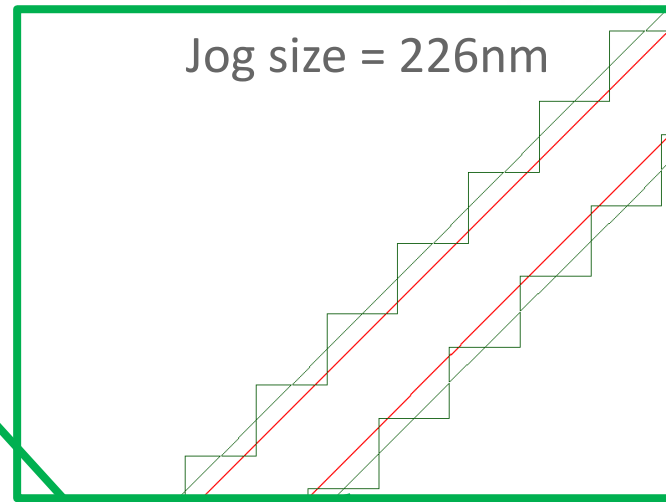
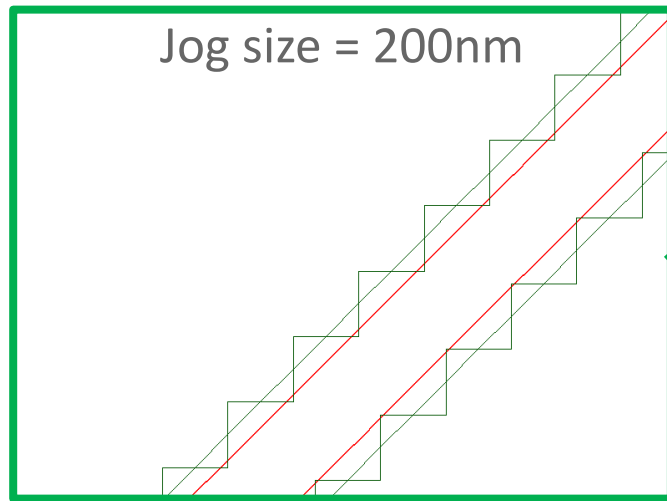
Majority of shots in this case are SRAFs, not main features  
SRAFs have little impact on wafer EPE

# Mask Wafer Co-Optimization (MWCO) Is the Key



# Small Jogs on Mask Filtered by Band-limited 193i Scanner

## -Use Bigger Shots & Simulation to Reduce Shot Count

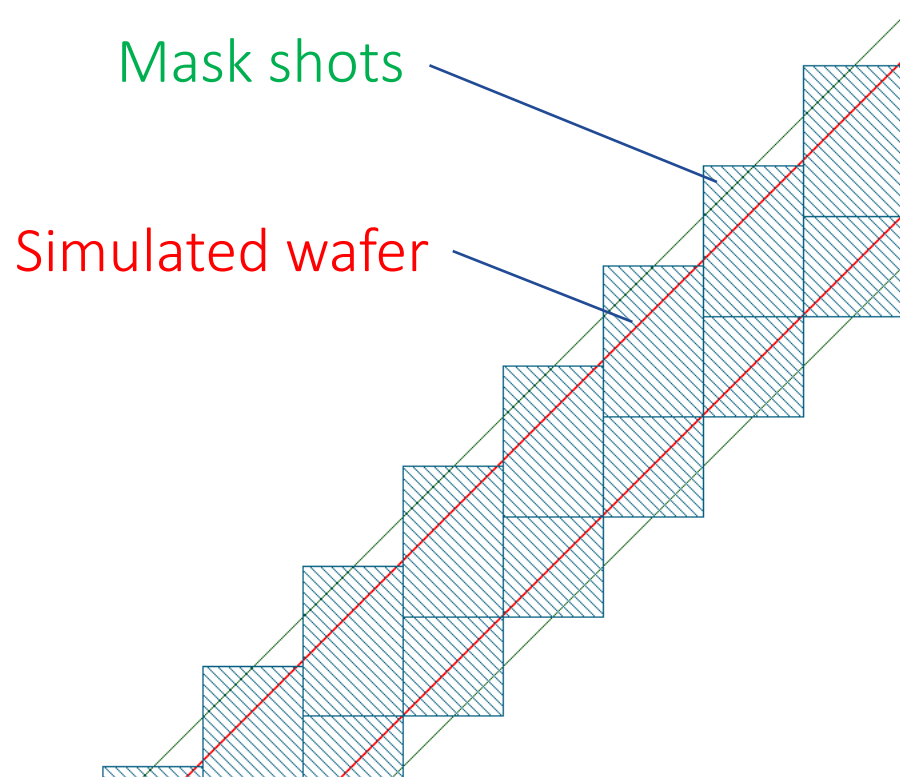




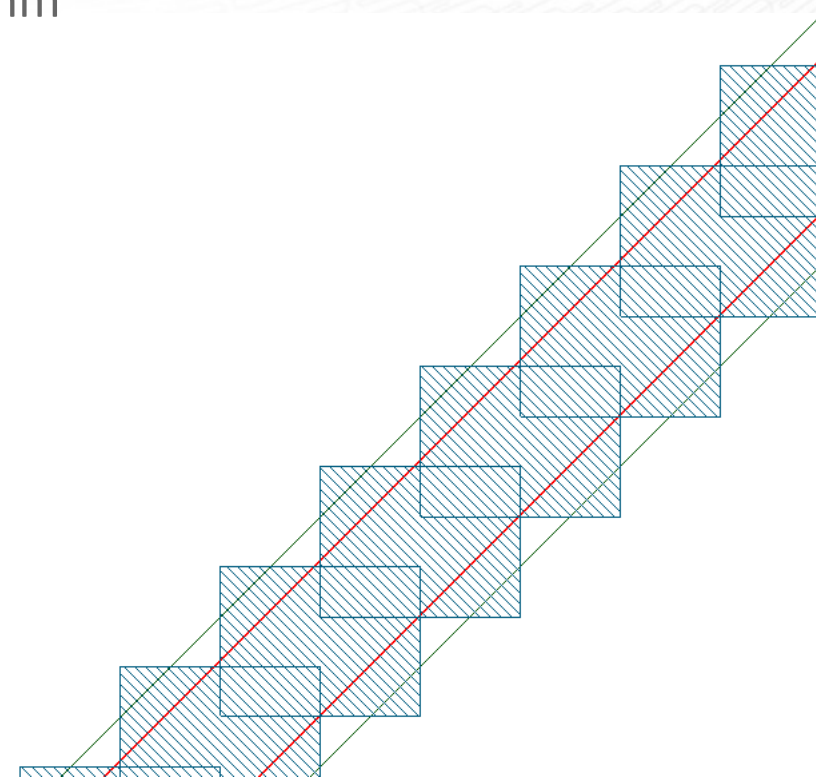
# Overlapping = Fewer Shots for Same Wafer EPE

- Use Overlapping Shots and Simulation to Reduce Shot Count

Jog size = 200nm



Conventional shots  
120 shots, wafer EPE = 0

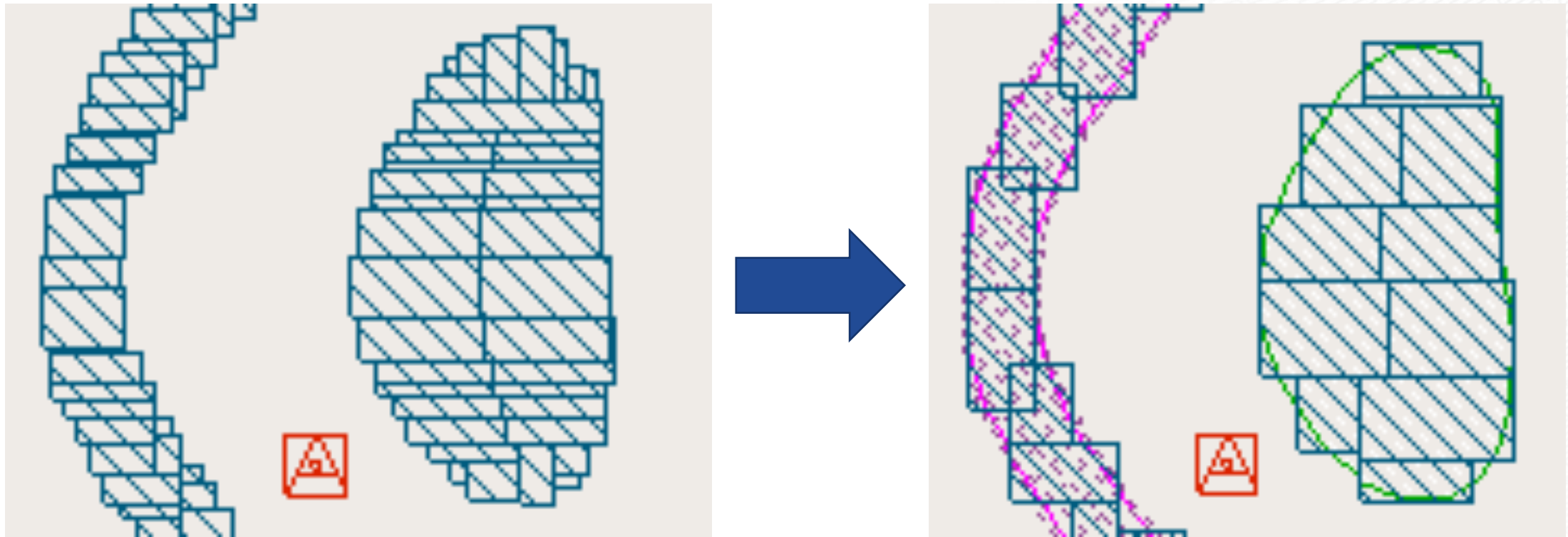


Overlapping shots  
64 shots, wafer EPE = 0



# Balance Shots for Write Time & Mask-Pattern Fidelity

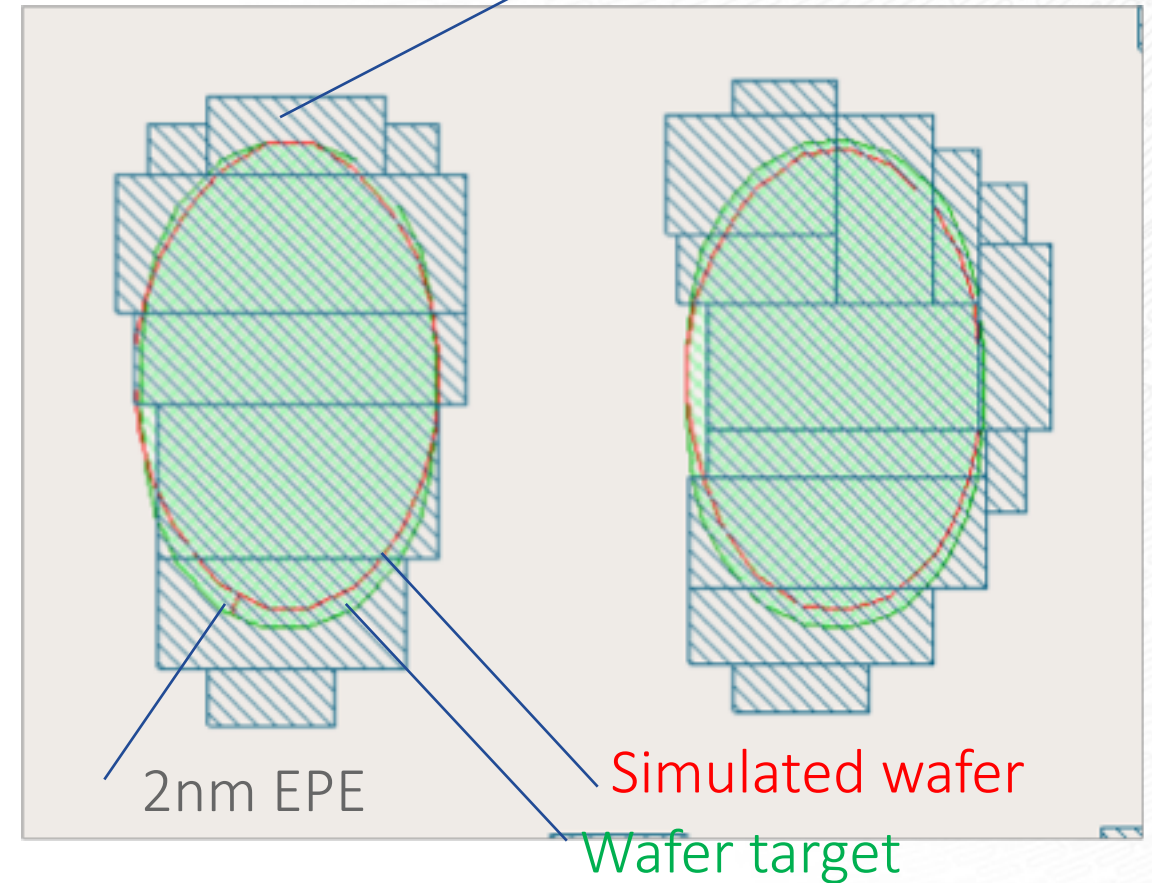
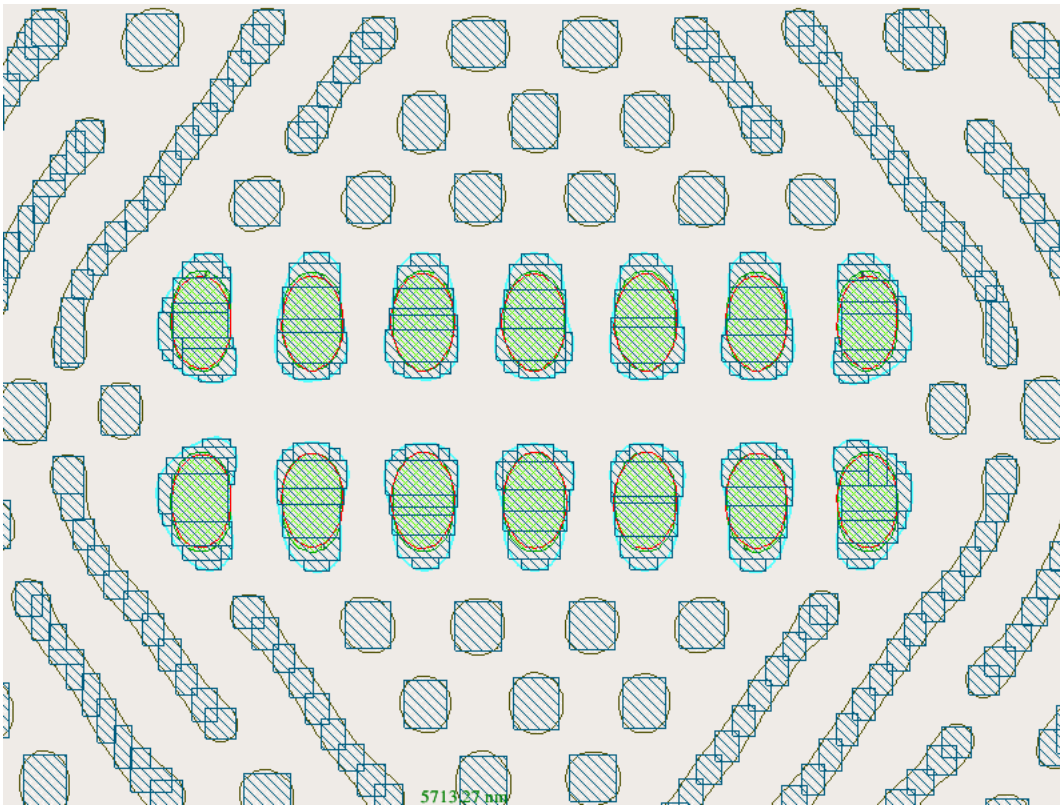
## Main Features: Conventional, SRAFs: Overlapping



# MWCO: The Key is to Minimize and Move Shots based on Simulation & Wafer EPE, not Mask Shape

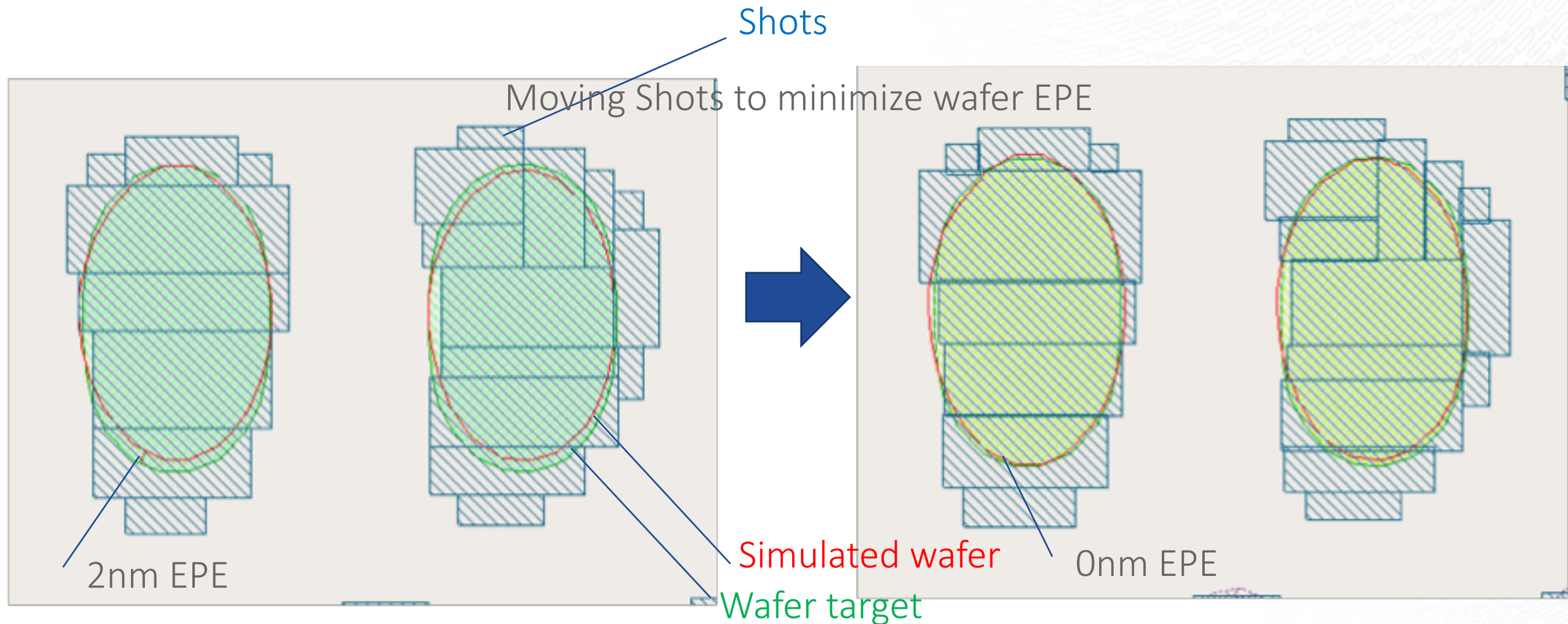
Generate Shots based on Mask EPE

Shots





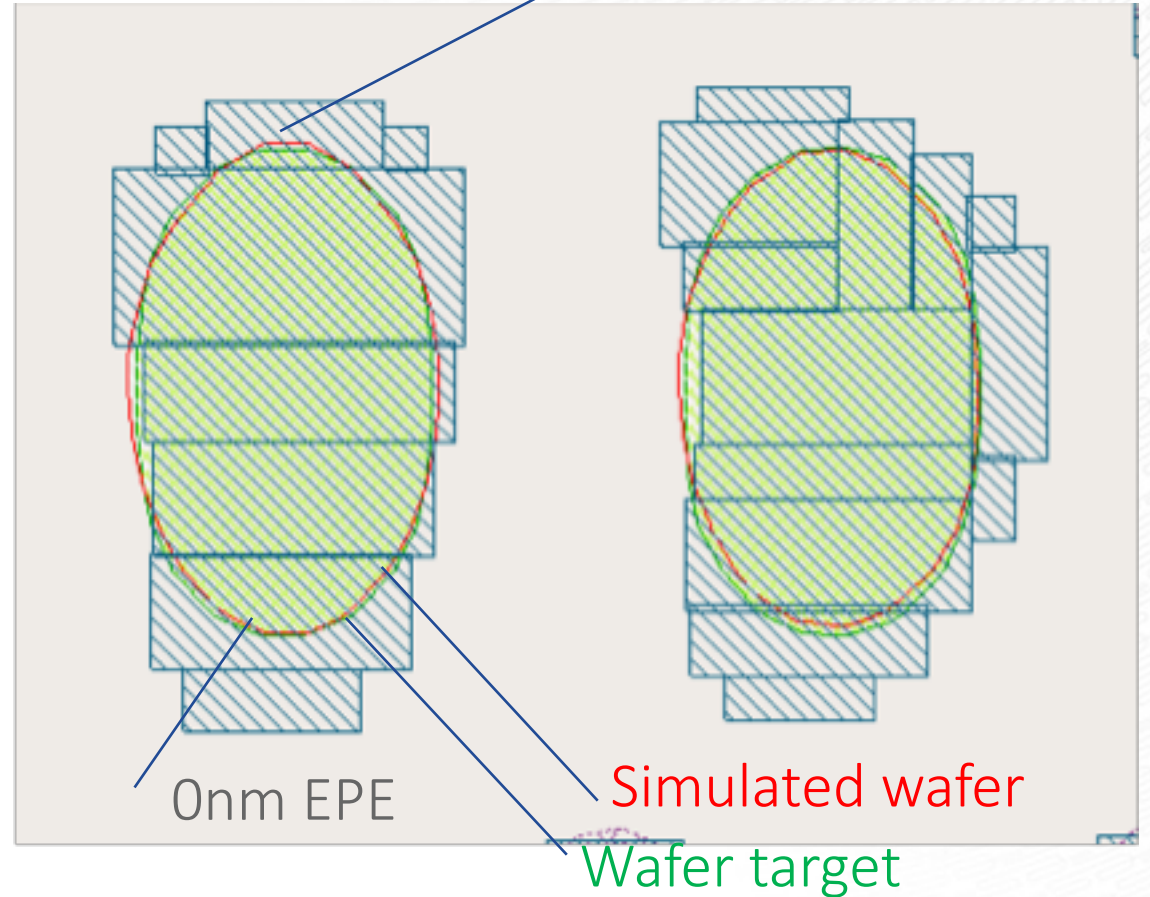
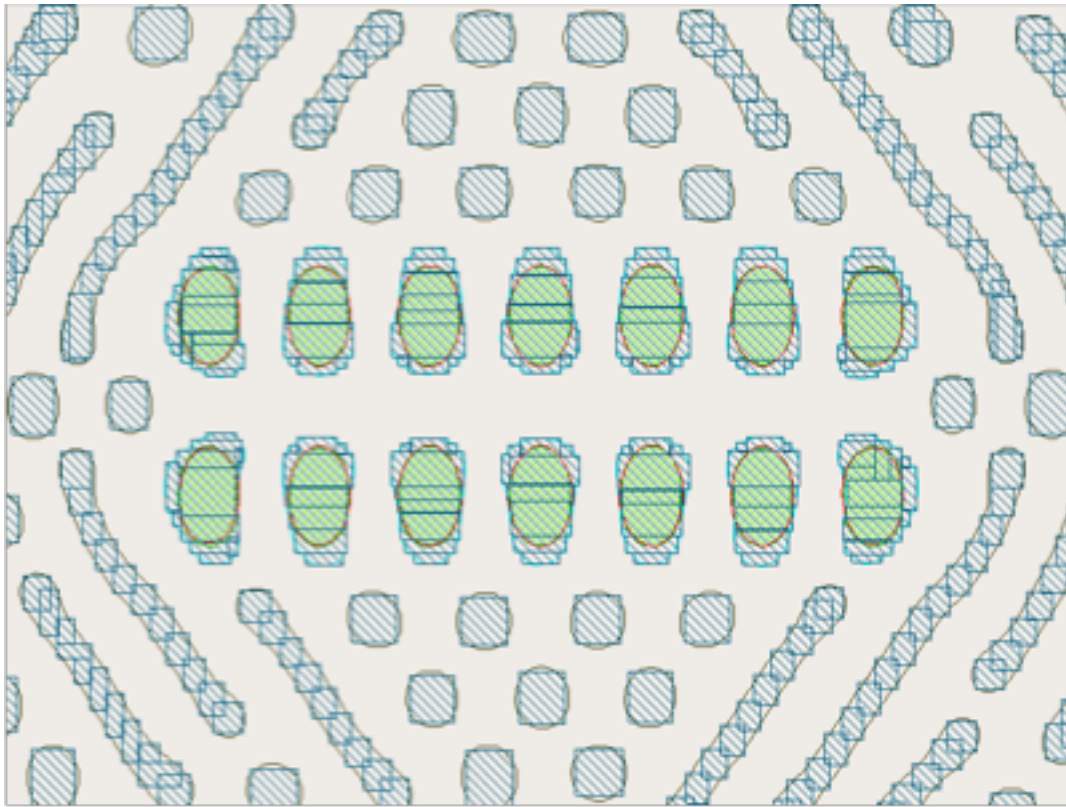
# MWCO: The Key is to Minimize and Move Shots based on Simulation & Wafer EPE, not Mask Shape



# MWCO: The Key is to Minimize and Move Shots based on Simulation & Wafer EPE, not Mask Shape

Optimize Shots based on wafer EPE

Shots

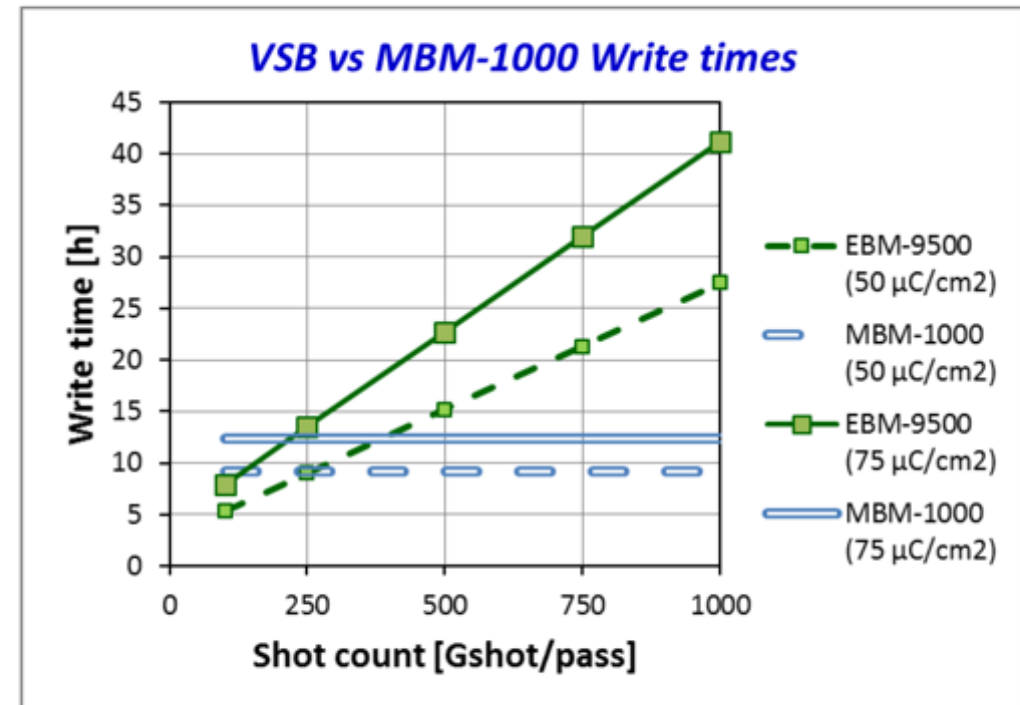




# VSB Writes Faster than Multi-Beam When Shot Density is Below 36 shots/ $\mu\text{m}^2$

Based on this NuFlare chart,  
if we want VSB writer to  
write a mask in less than 12  
hours, the average shot  
density should be <36  
shots/ $\mu\text{m}^2$

✦ MB is advantageous with shot counts > ~200 Gshot/pass.



NUFLARE

June 22, 2016

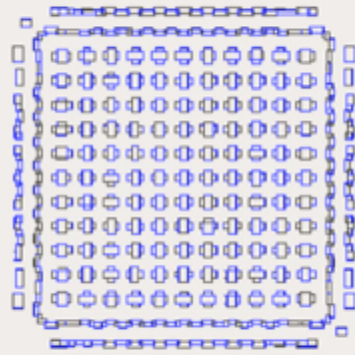
eBeam Initiative Taiwan seminar

13

D2S

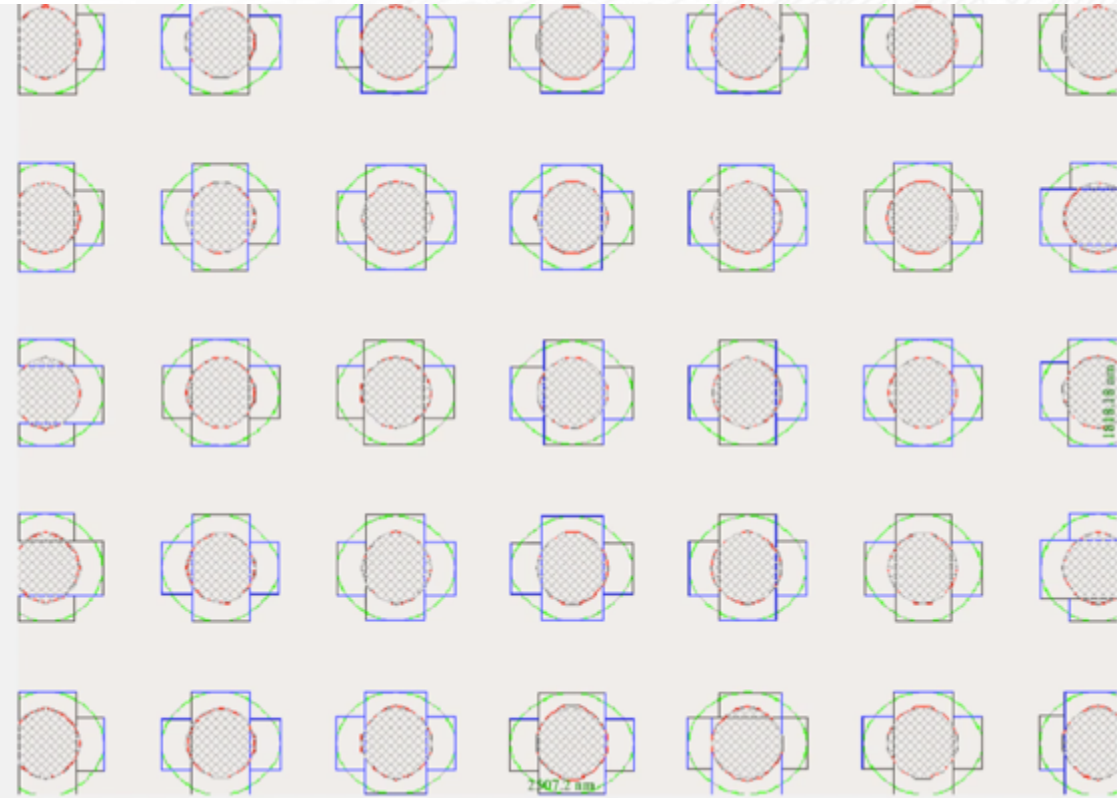


# Let's Evaluate Reduced Shot Count of MWCO Across Entire Chip Design Space – From Dense to Isolated



18.1076 um

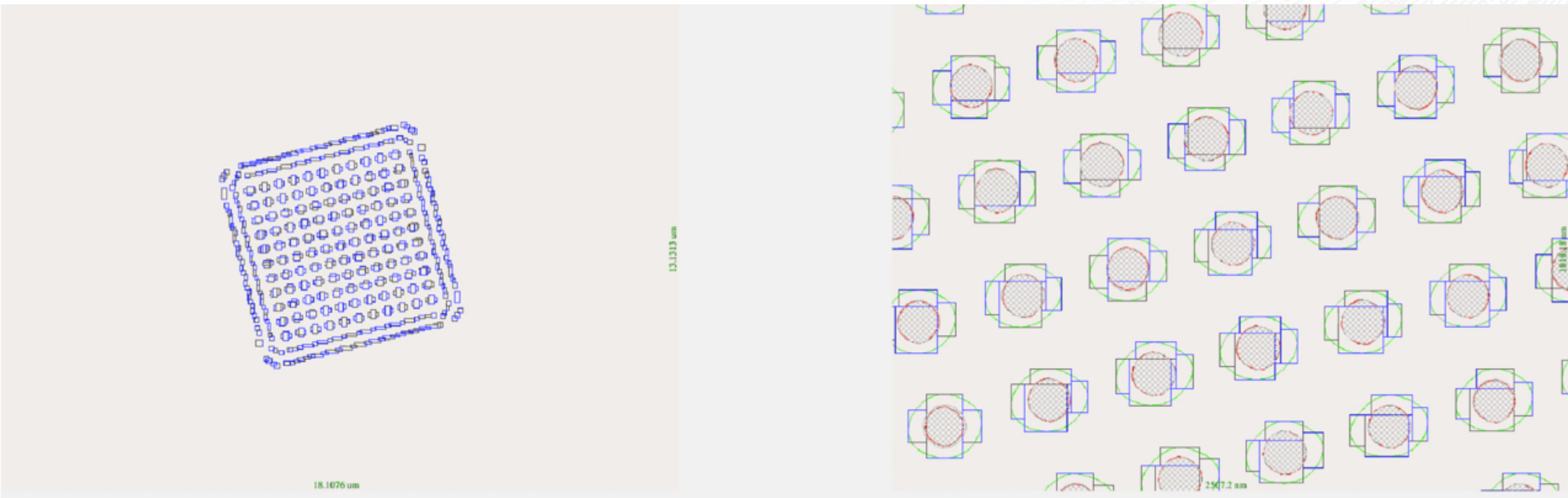
13.1313 um



18.1076 um



# Let's Evaluate Reduced Shot Count of MWCO Across Entire Chip Design Space – From Dense to Isolated

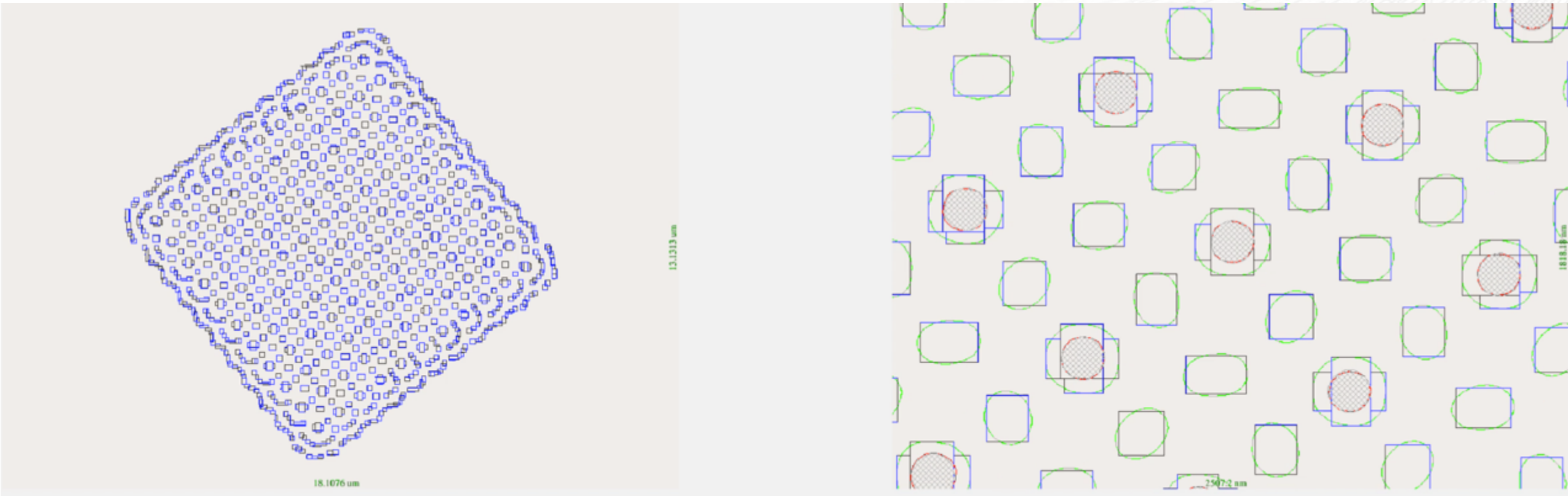


# Let's Evaluate Reduced Shot Count of MWCO Across Entire Chip Design Space – From Dense to Isolated

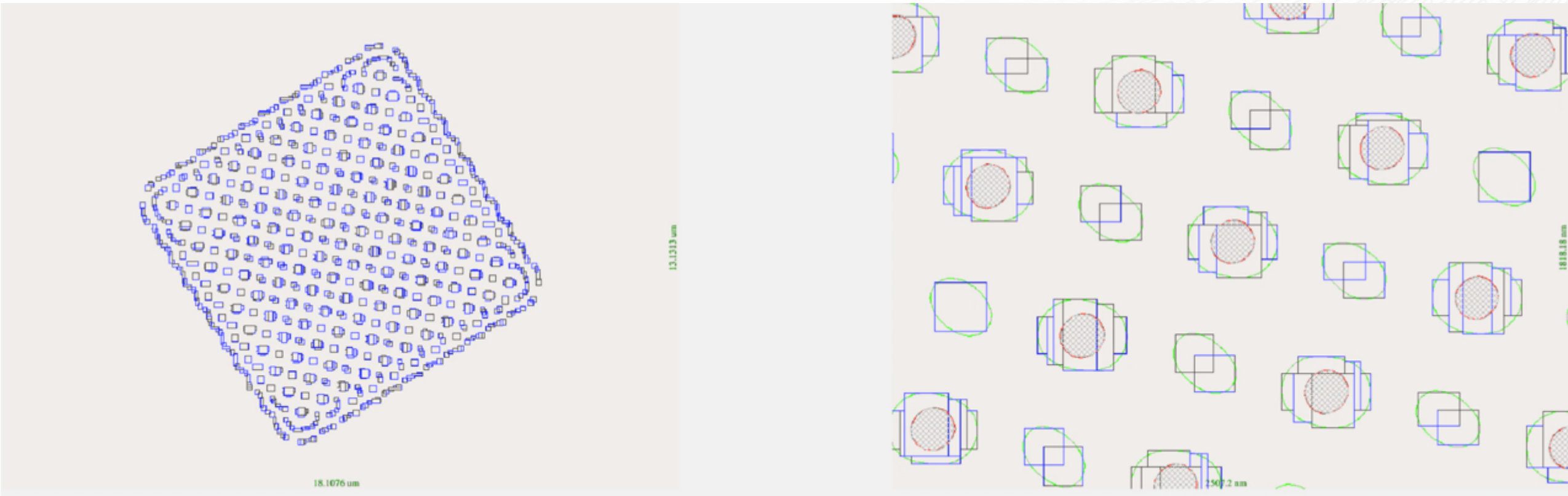




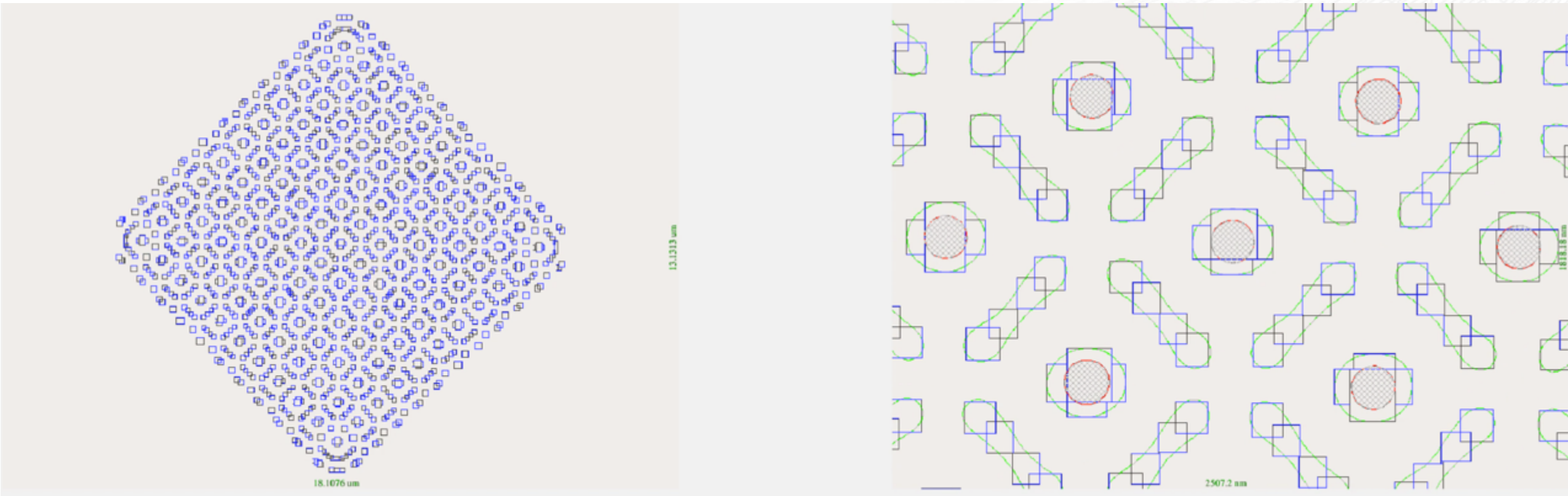
# Let's Evaluate Reduced Shot Count of MWCO Across Entire Chip Design Space – From Dense to Isolated



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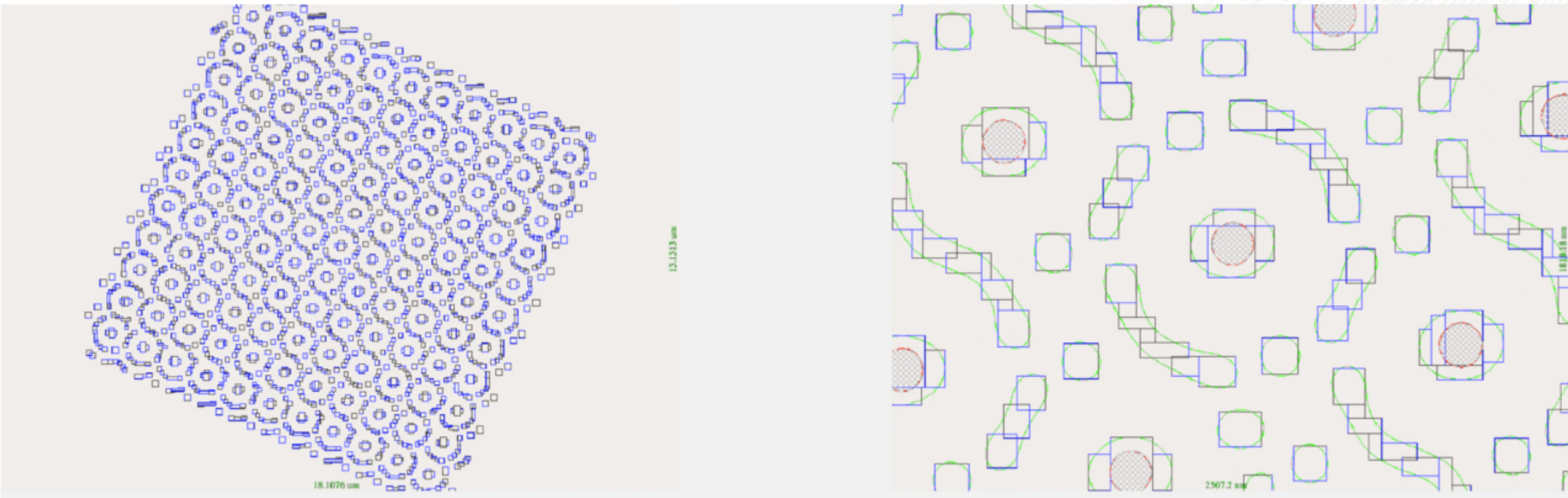


# Let's Evaluate Reduced Shot Count of MWCO Across Entire Chip Design Space – From Dense to Isolated

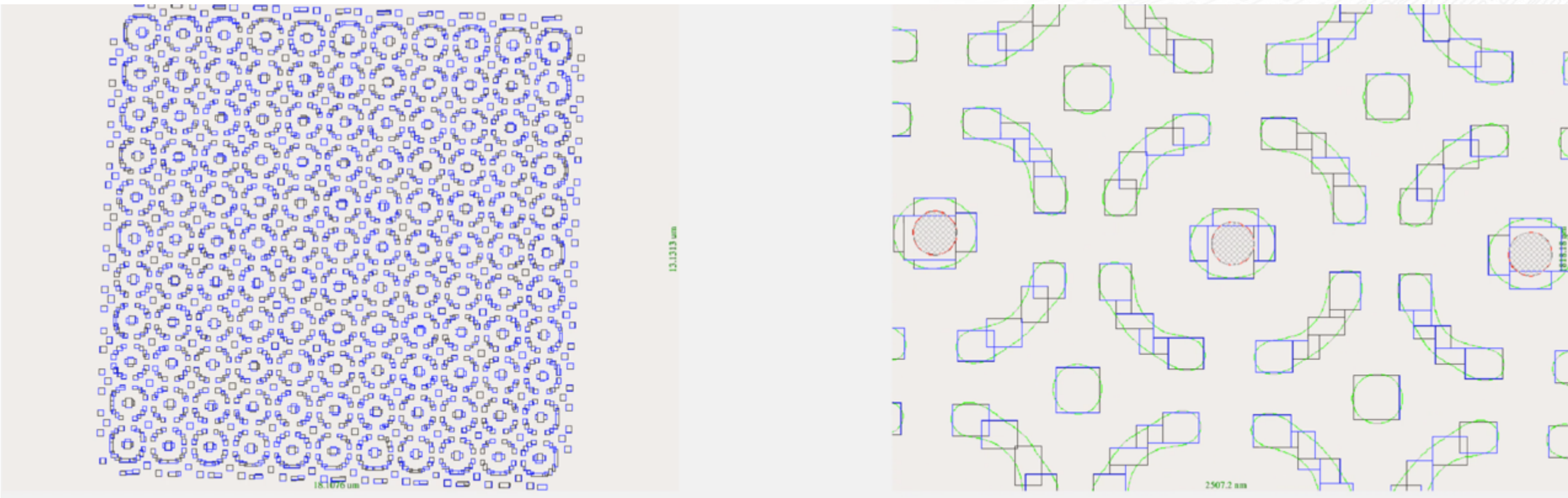




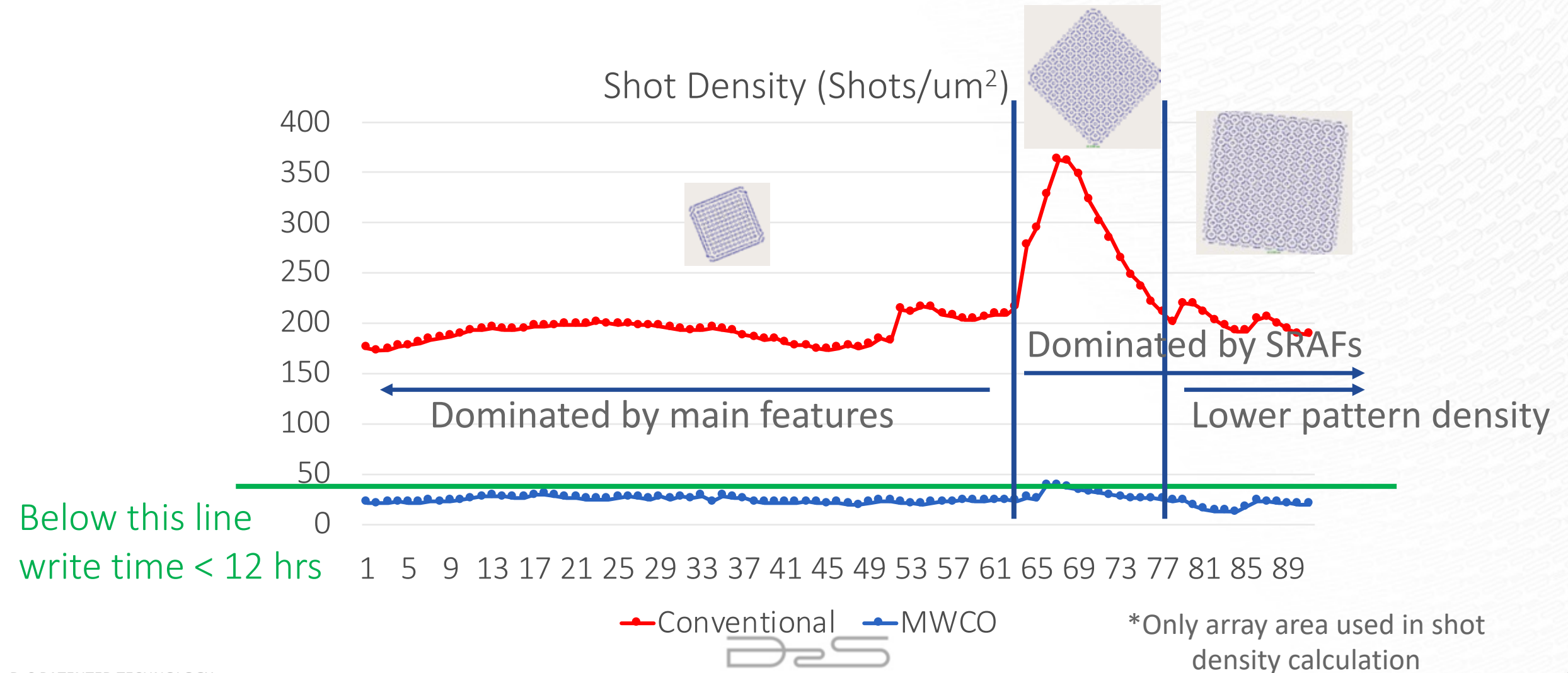
# Let's Evaluate Reduced Shot Count of MWCO Across Entire Chip Design Space – From Dense to Isolated



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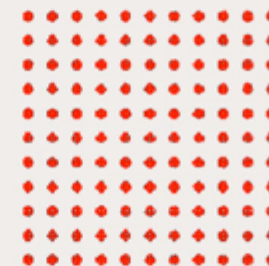
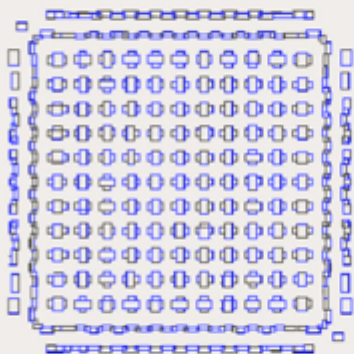


# Full Curvilinear ILT Mask w' MWCO can be Written within 12 Hrs on VSB Writer – Less Write Time than Multi-Beam





# TrueMask® ILT MWCO: Full-Chip Curvilinear ILT in a Day & VSB Writing in 12 hours for 193i

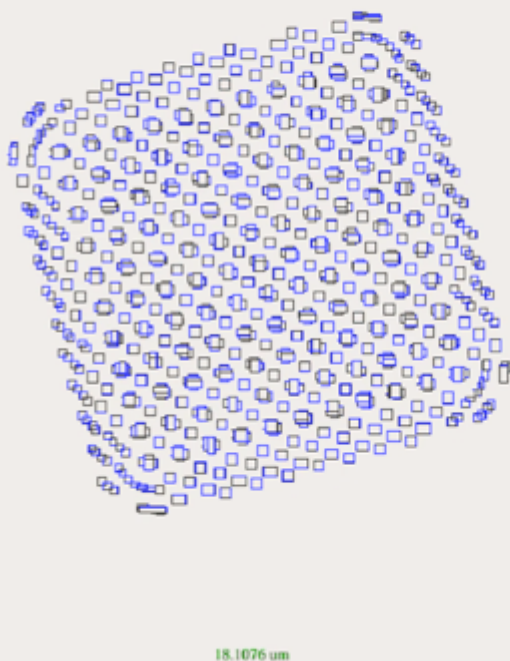


TrueMask ILT curvilinear mask VSB shots  
for different pitches & orientations

Corresponding simulated wafer  
print



# TrueMask® ILT MWCO: Full-Chip Curvilinear ILT in a Day & VSB Writing in 12 hours for 193i



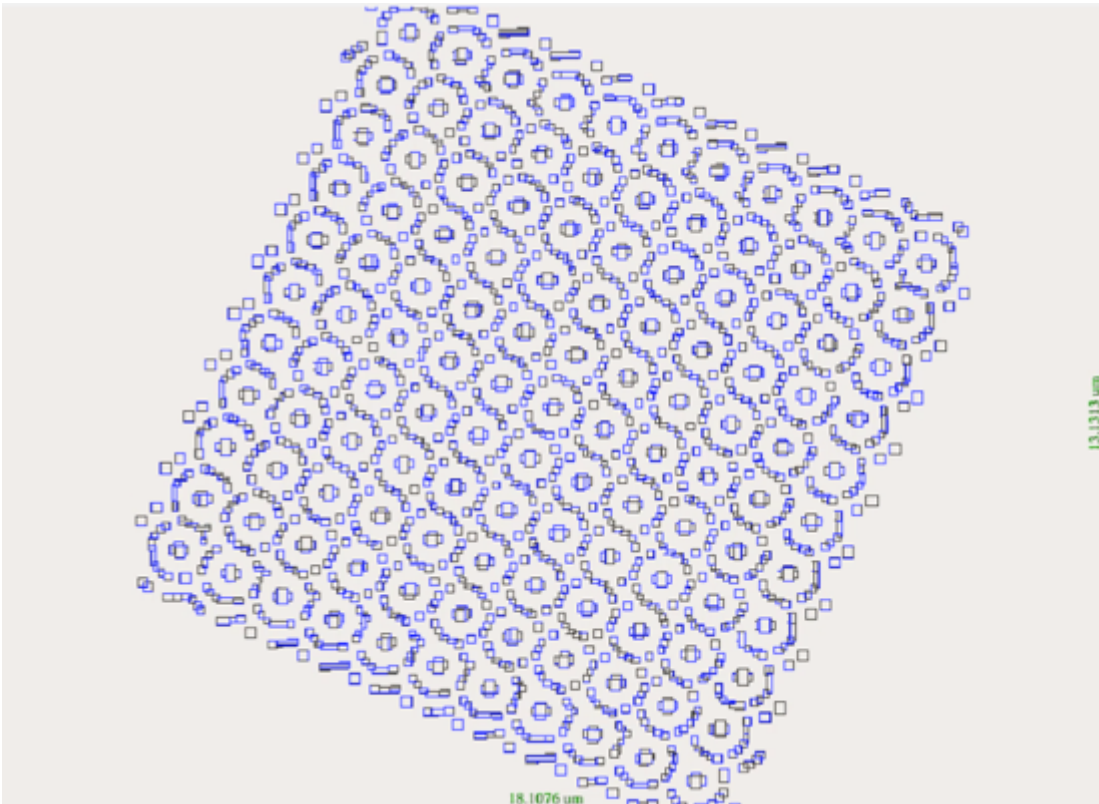
TrueMask ILT curvilinear mask VSB shots  
for different pitches & orientations



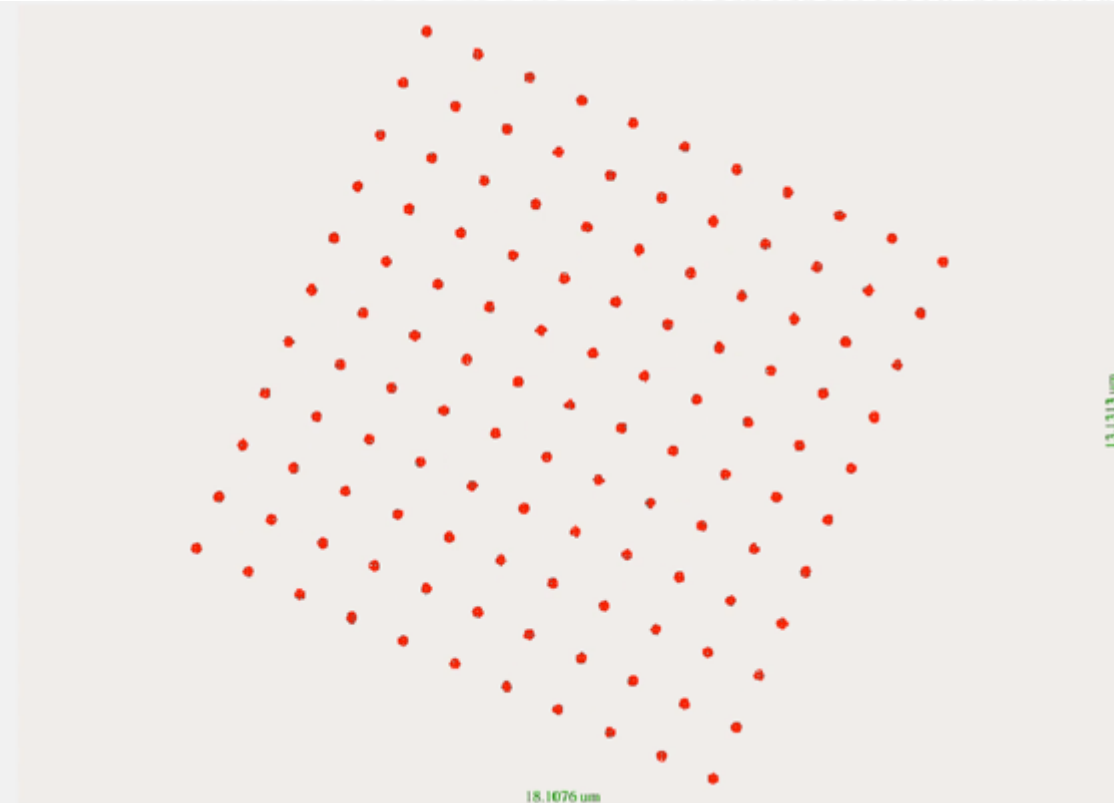
Corresponding simulated wafer  
print



# TrueMask® ILT MWCO: Full-Chip Curvilinear ILT in a Day & VSB Writing in 12 hours for 193i



TrueMask ILT curvilinear mask VSB shots  
for different pitches & orientations

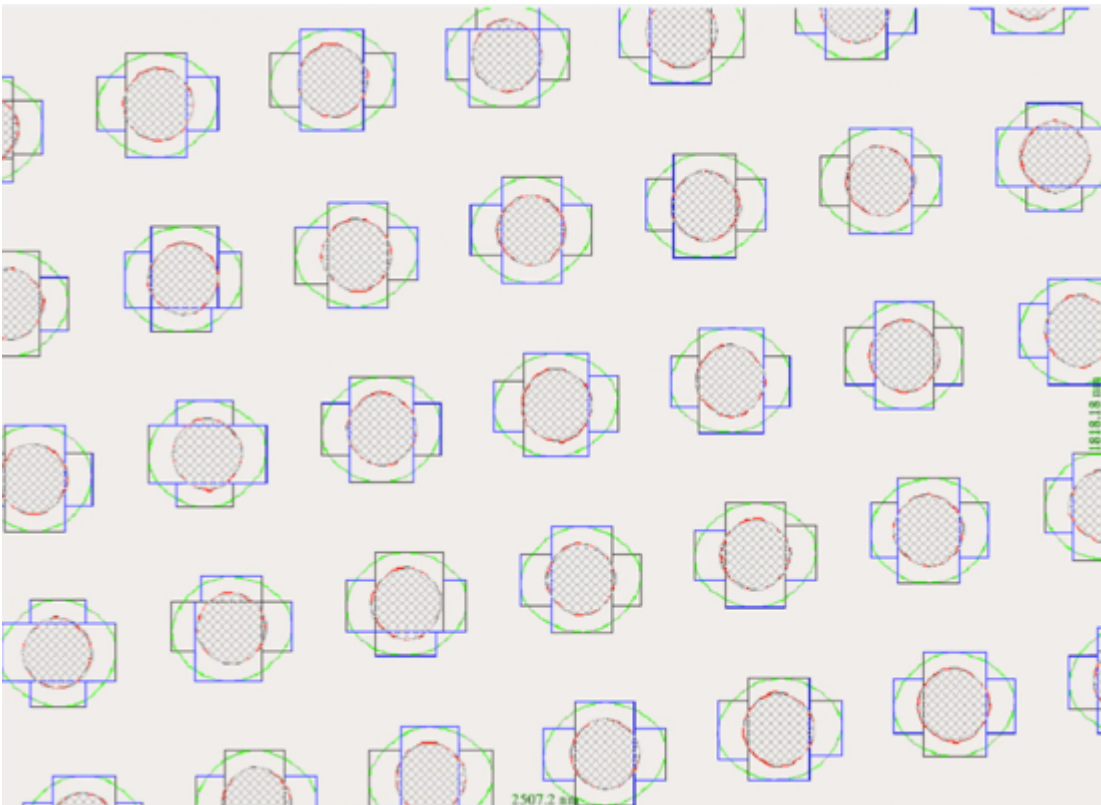


Corresponding simulated wafer  
print

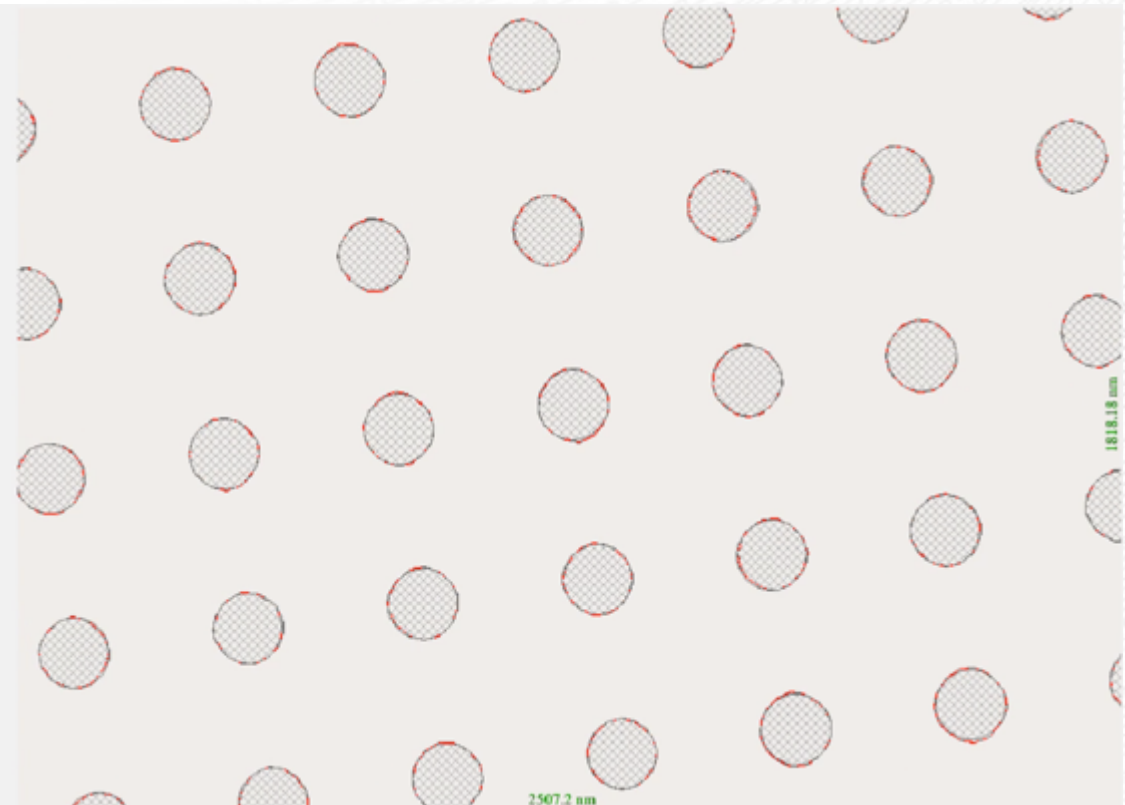




# TrueMask® ILT MWCO: Full-Chip Curvilinear ILT in a Day & Full Mask Multi-Beam and VSB Writing in 12 hrs for 193i



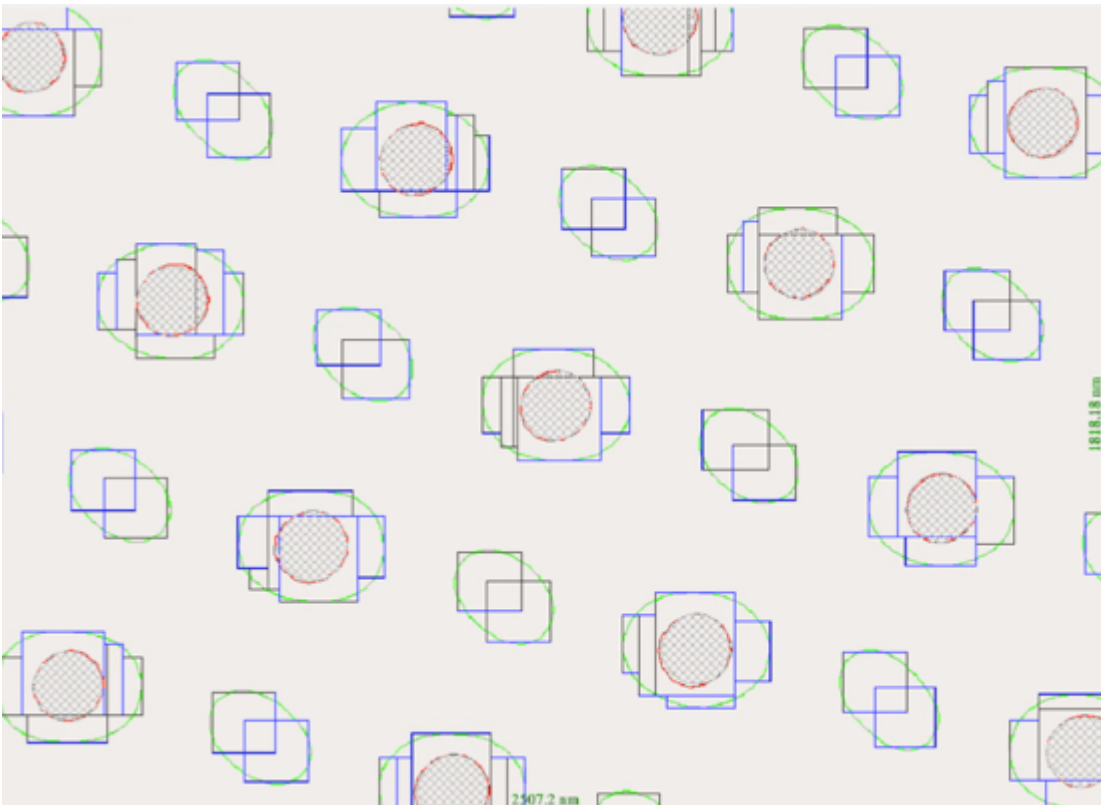
TrueMask ILT curvilinear mask VSB shots for different pitches & orientations



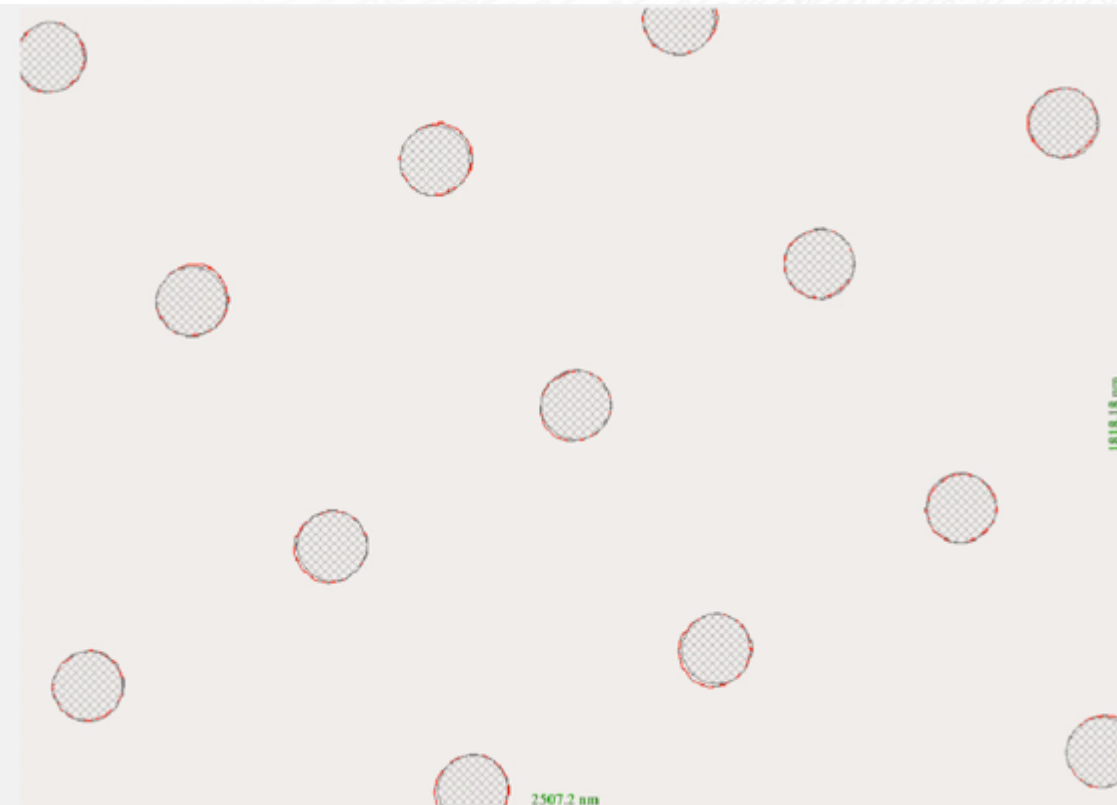
Corresponding simulated wafer print



# TrueMask® ILT MWCO: Full-Chip Curvilinear ILT in a Day & Full Mask Multi-Beam and VSB Writing in 12 hrs for 193i



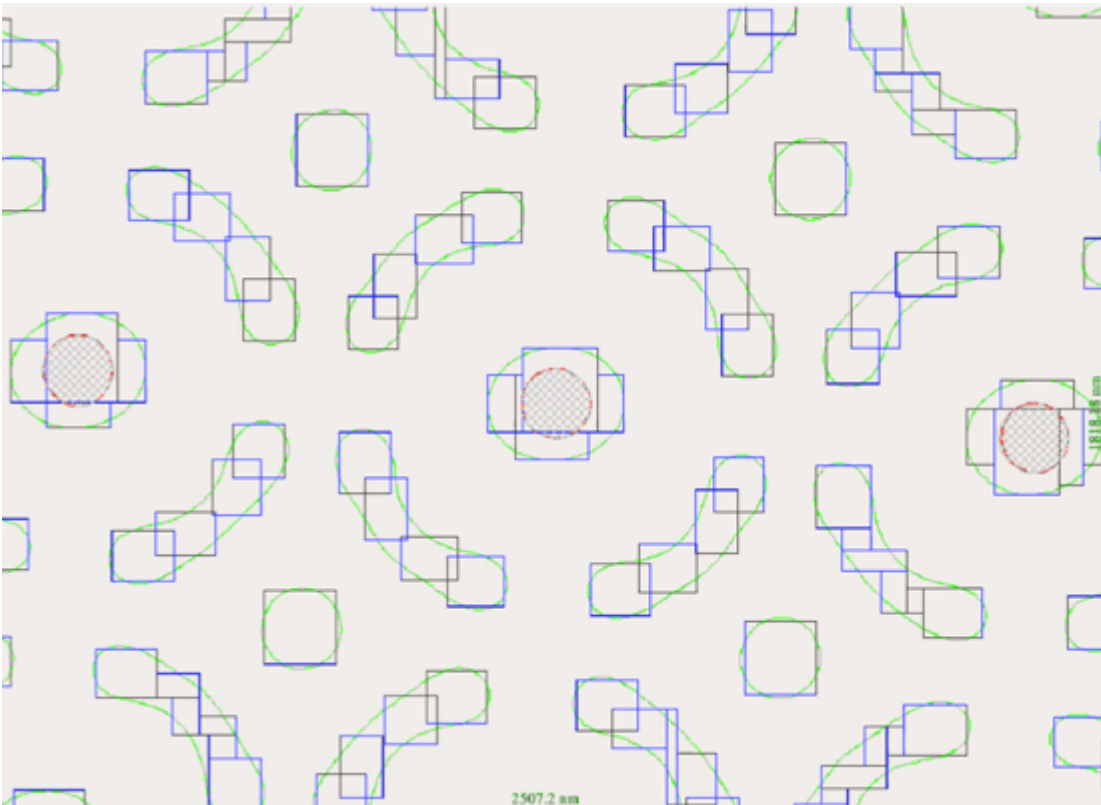
TrueMask ILT curvilinear mask VSB shots  
for different pitches & orientations



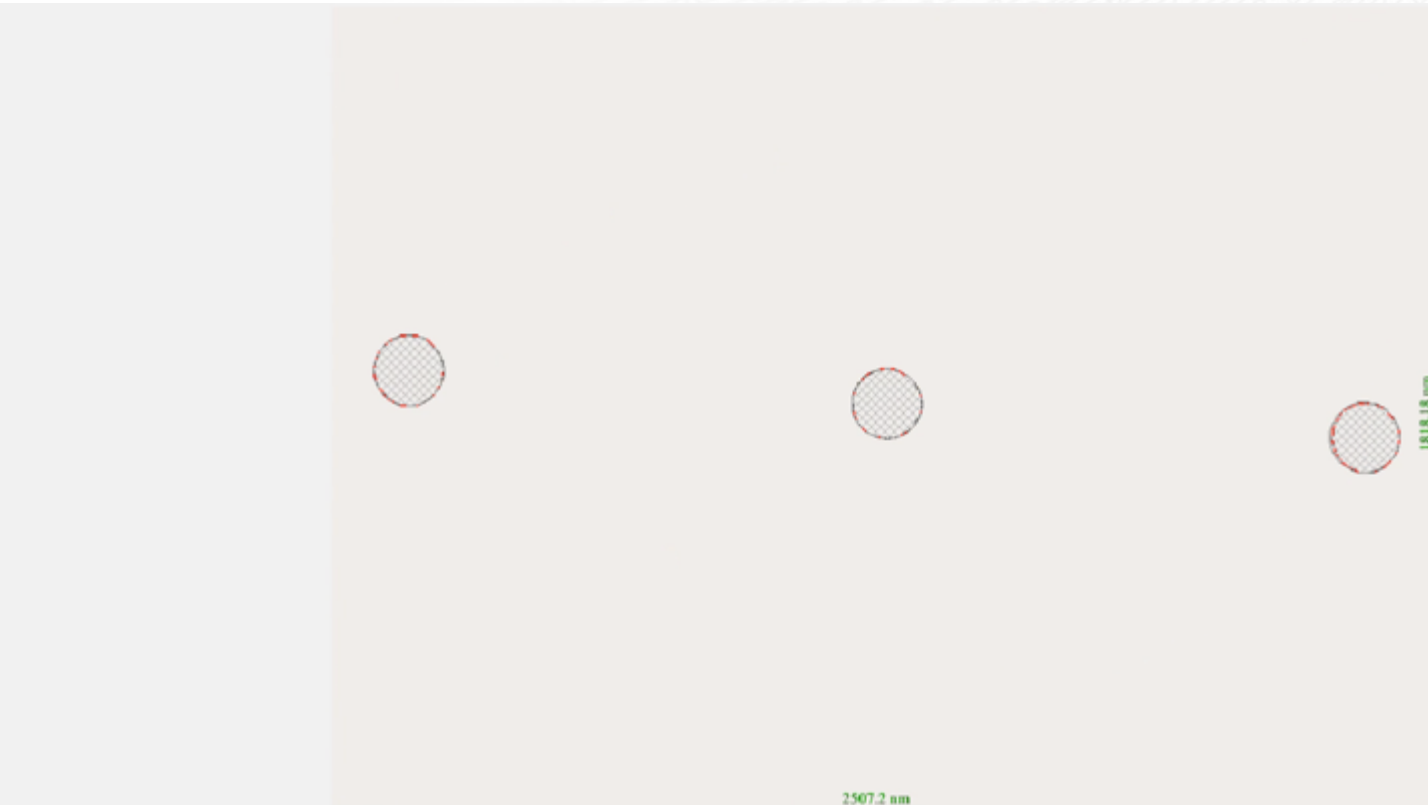
Corresponding simulated wafer  
print



# TrueMask® ILT MWCO: Full-Chip Curvilinear ILT in a Day & Full Mask Multi-Beam and VSB Writing in 12 hrs for 193i



TrueMask ILT curvilinear mask VSB shots for different pitches & orientations



Corresponding simulated wafer print







Thanks to NuFlare for their help to write the  
curvilinear masks with MBM-1000



Thanks to ASML for their help to acquire wafer  
images with eP5 platform