July 11, 2022| AKI FUJIMURA, CEO, D2S, Inc.

Is Curvy Design an Opportunity, or a Dream?

Today's GPU Workstation = 8,000 Cray-2s

60,000,000x Price Performance

It's time to rethink EDA

Cray-2 (1985)
1.9 GFLOPS w/500MB @ $15M

nVIDIA RTX 3090 Ti (2021)
15,300 GFLOPS w/24GB @ $2,000

Computation Choices Impact Execution Choices

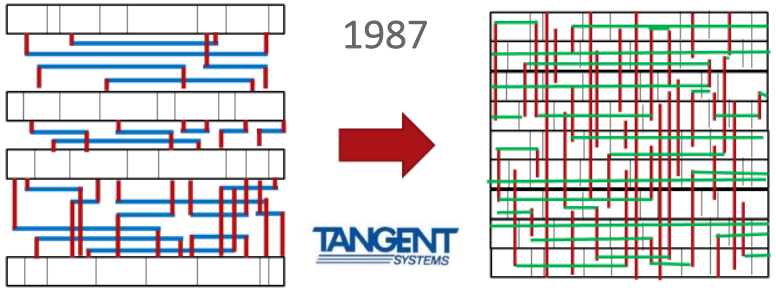
Today's Semiconductor Design Choices

Minecraft, Mojang (Microsoft)

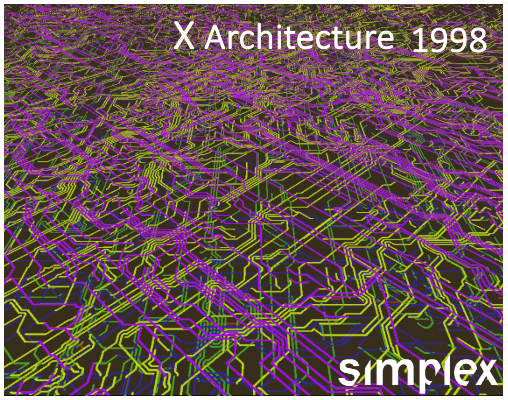
The Future Semiconductor Design Could Choose Now

Death Stranding, Kojima Productions

Once Upon a Time, Rectangles Served a Purpose



DEF, LEF, ECO, …



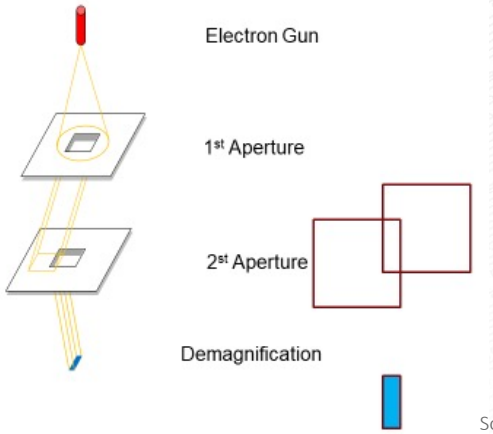
Edge-based, Manhattan design assumptions made design easier, and most importantly, were a practical fit for the computation available at the time

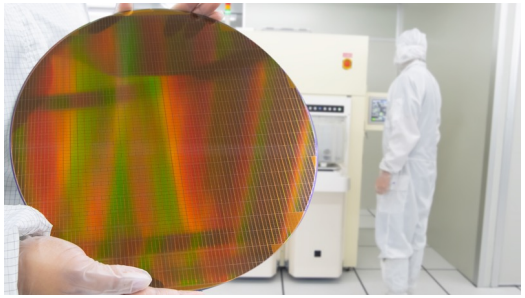
But times (and computing) have changed…

Wafers are Exposed by Masks

photomask

Variable Shaped Beam (VSB) Mask Writing



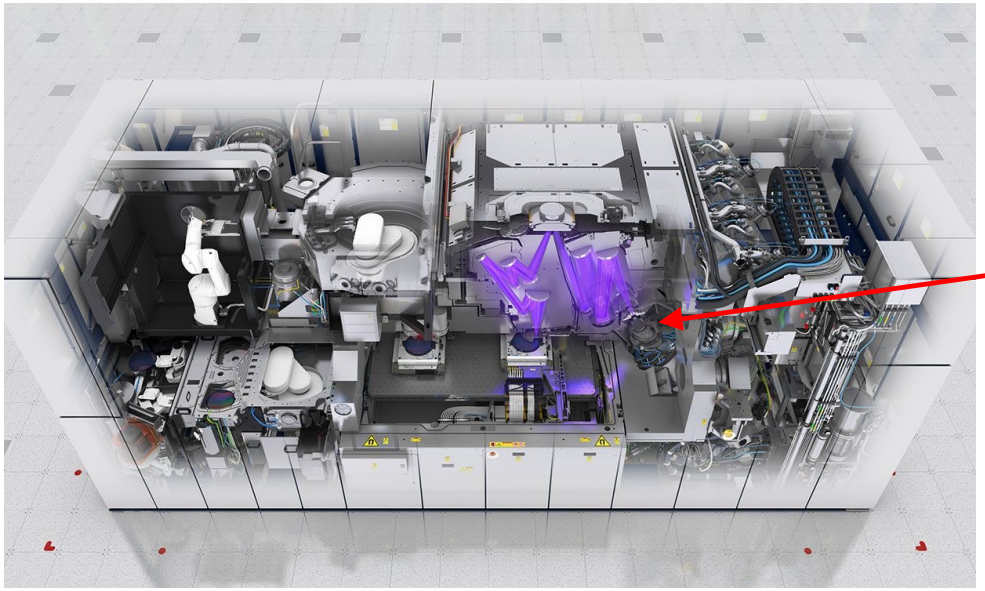


Resolution of 193i =

$$\frac{193\text{nm wavelength}}{1.35\text{ Numerical Aperture}}$$

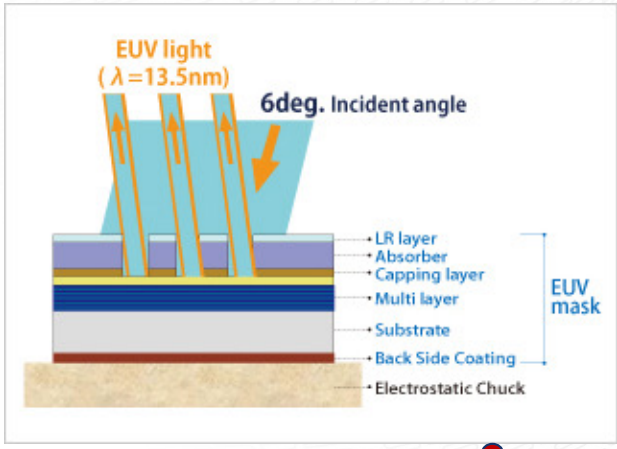
Source: ASML

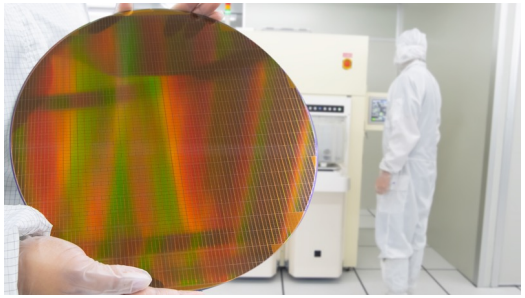
EUV: Still Wafers are Exposed by Masks



Source: ASML

EUV mask

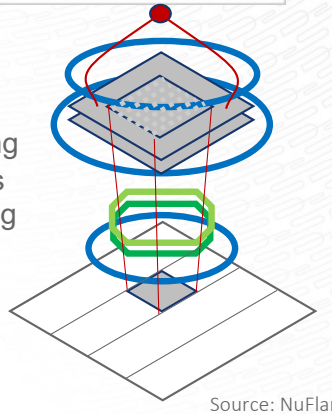




Resolution of EUV =

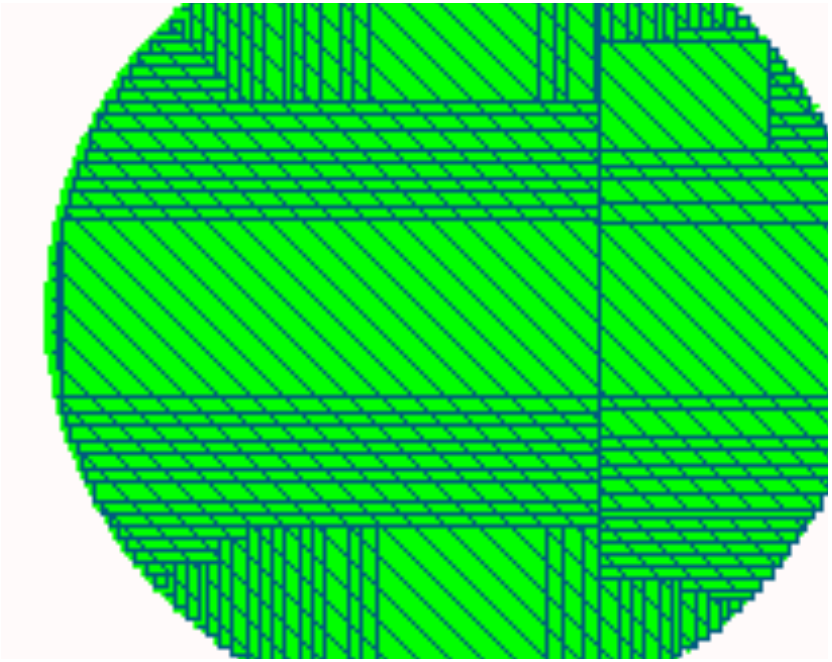
$$\frac{\text{13.5nm wavelength}}{\text{0.33 Numerical Aperture}}$$

Multi-Beam Mask Writing
256K square apertures
for electron beam writing
of masks

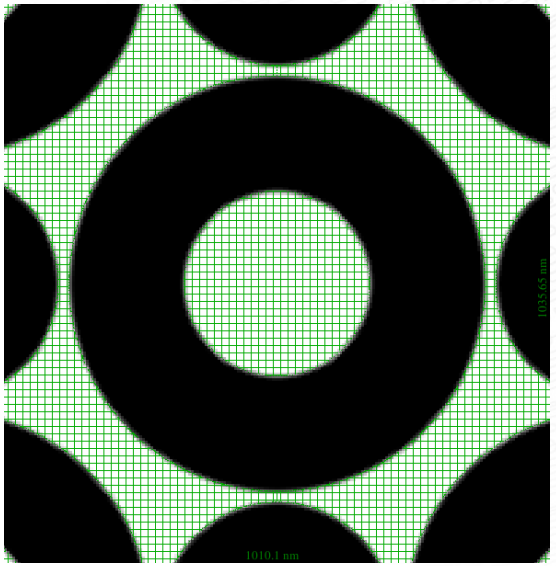


Source: NuFlare

Multi-beam Mask Writing Has Enabled Curvy Masks



- Generates too many shots
- Takes too long to write



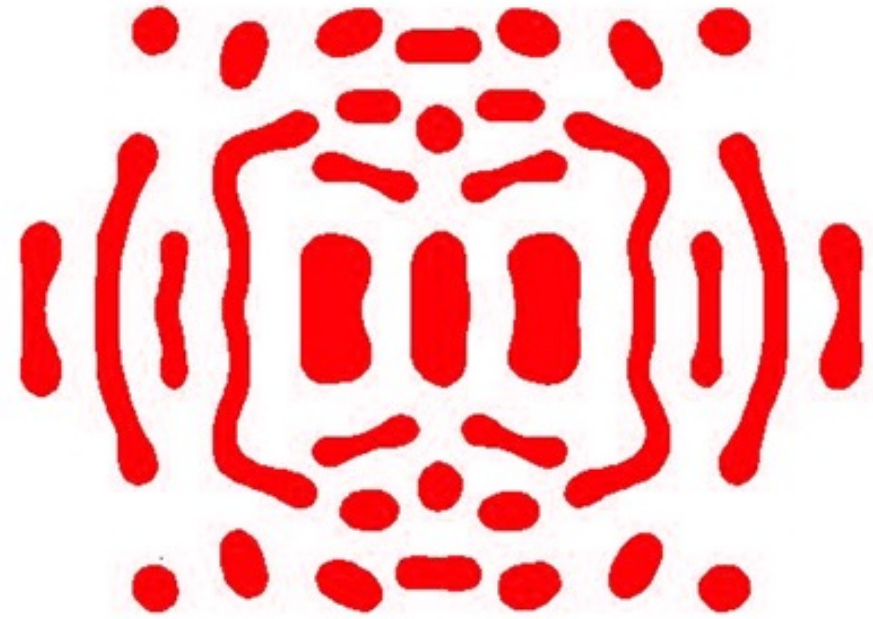
Multi-beam mask writer

- Designed for curvilinear ILT
- Writes any shape in constant time

ILT is Software that Computes Mask Shapes

Generates Curvilinear Masks for Multi-beam Writing

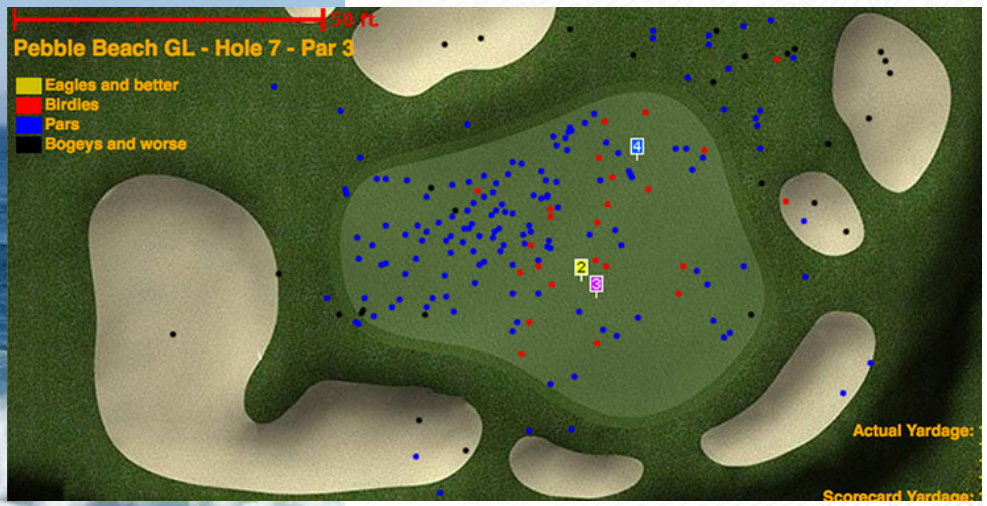
Design (Wafer Target)



Curvilinear ILT (Mask Target)

Key to Manufacturing is Resilience to Variation

Shortest hole on PGA Tour is a Difficult Par 3

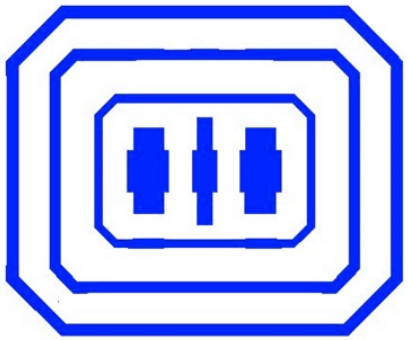


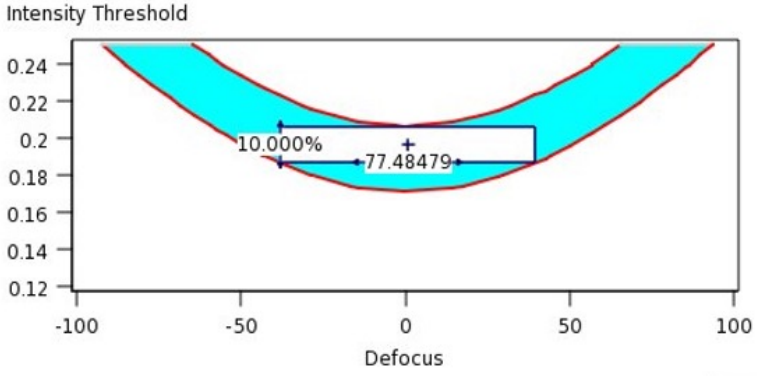
Shot Dispersion of Pros in 2016
25 birdies; 153 pars; 32 bogeys; 8 Doubles

Curvy Masks: More Resilient to Manufacturing Variation

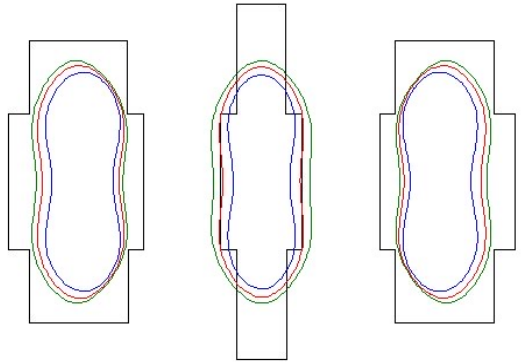
Curvilinear ILT vs. Standard OPC: *First-to-fail site*

Standard OPC

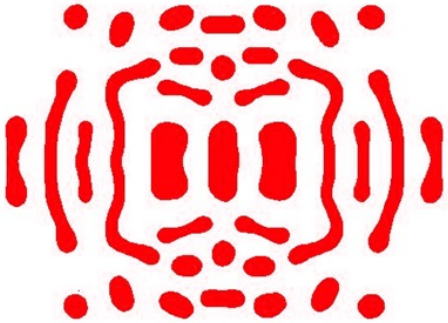




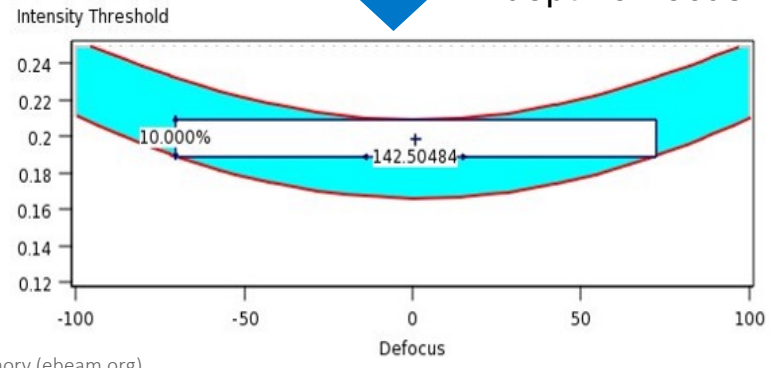
PV Band
0, 60, 90nm defocus

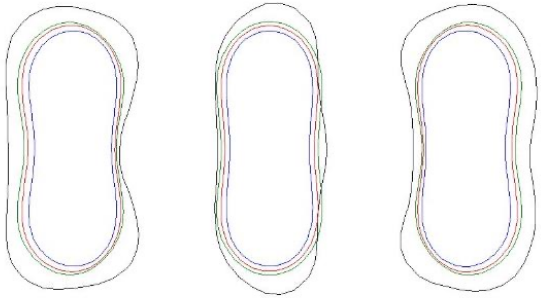


Curvilinear ILT



~85% increase in depth of focus

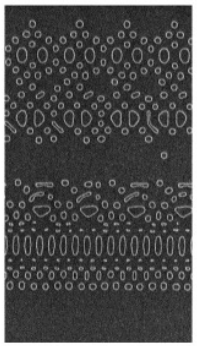


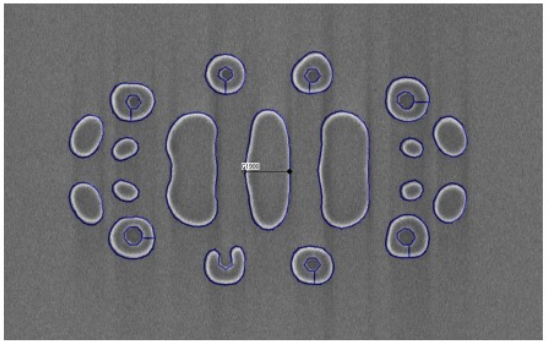


Source: Micron, ILT Curvilinear Mask Designs for Advanced Memory (ebeam.org)

Manufacturing Now Enables New Choices: Curvilinear Masks Are Here Today

Micron Shows Curvilinear ILT Mask Written by NuFlare Multi-Beam Writer MBM-1000 with High Pattern Fidelity





Blue outline = Mask Data

- Pattern fidelity is not a concern, even with aggressive AFs
- In collaboration with NuFlare and D2S: written on MBM-1000

Overlay of Mask Data and Mask SEM

11

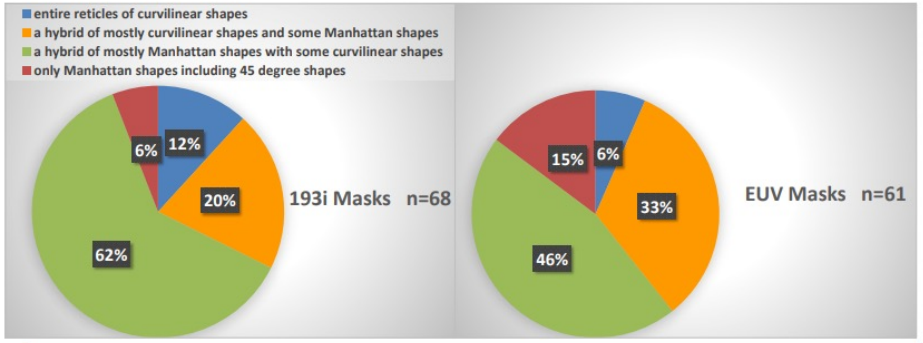
Micron
Ezequiel Russell

Curvilinear Shapes to be Pervasive by 2023

94% of 193i, 85% of EUV masks with some curvilinear shapes

eBeam Initiative

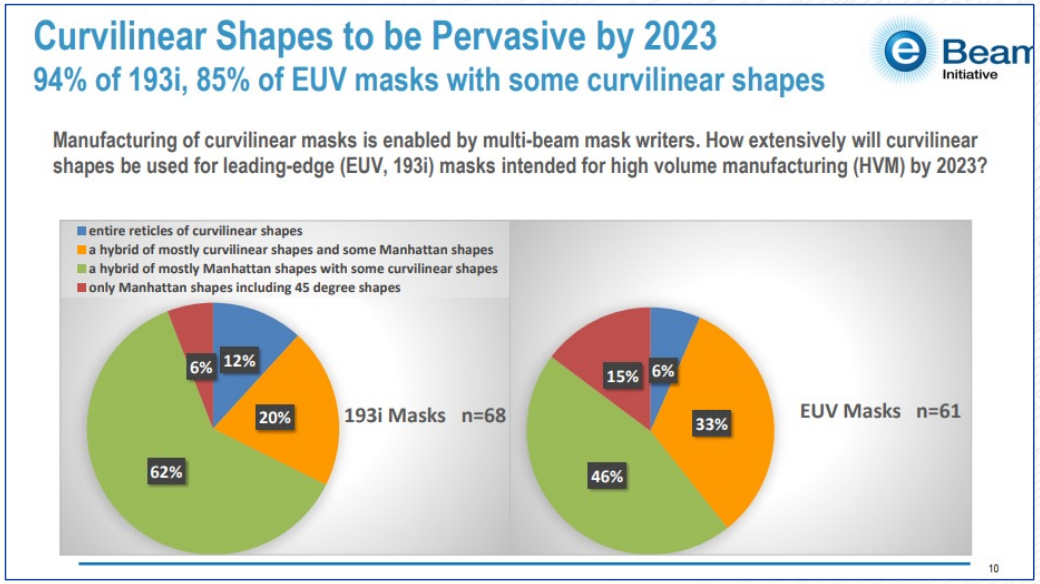
Manufacturing of curvilinear masks is enabled by multi-beam mask writers. How extensively will curvilinear shapes be used for leading-edge (EUV, 193i) masks intended for high volume manufacturing (HVM) by 2023?



10

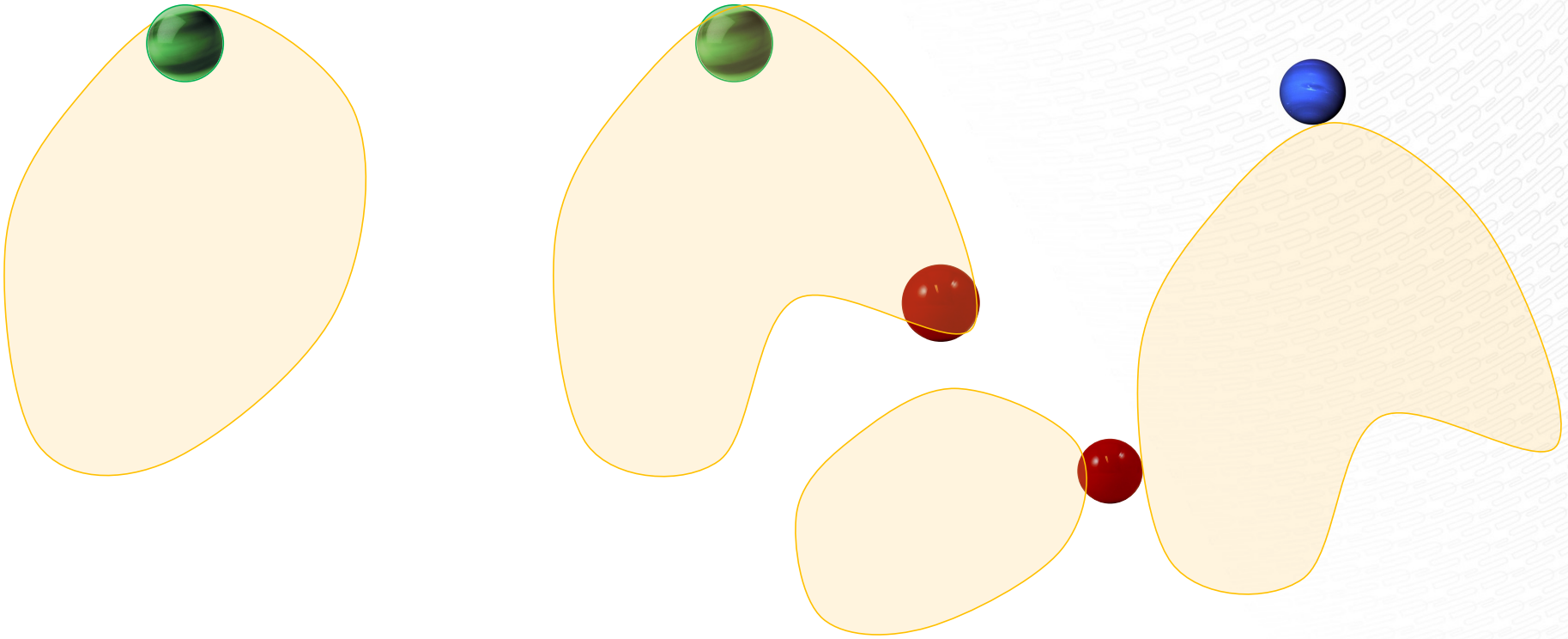
Both 193i and EUV Will Use Curvy Masks

- Masks are written by data
- Wafers are written by masks
- Curvy masks can be written just as accurately and just as quickly for the same cost:
  - Curvy data format with SEMI
  - Pixel-based GPU-accelerated datapath for:
    - Mask process correction (MPC)
    - Mask rules check (MRC)



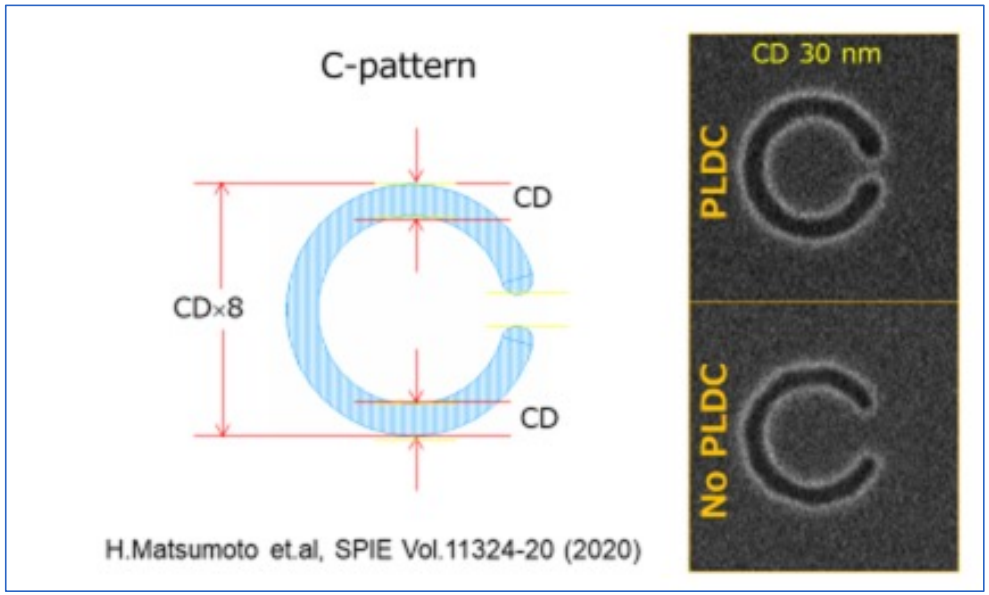
Manufacturing Has Been Trailblazing:

Curvy MRC Shows Simplified Curvy DRC is Known-Feasible



Pearman, et al, PMJ 2019

Manufacturing Has Been Trailblazing:
Mask Process Correction and Bias In Pixel Domain



- NuFlare's Multi-Beam Mask Writer has:
  - Linearity Correction including for Curvy Masks
  - Edge Enhancement including for Curvy Masks
  - Every pixel enhanced
  - Real time while writing (only possible inline w/GPU)
- For masks, everything is handled flat, too
- So, we know that similar things in the wafer design domain are also feasible

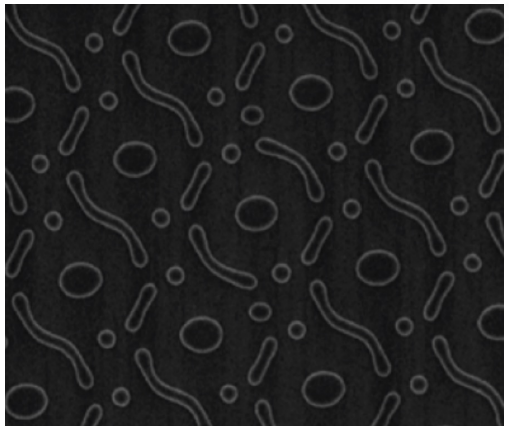
NuFlare

D2S

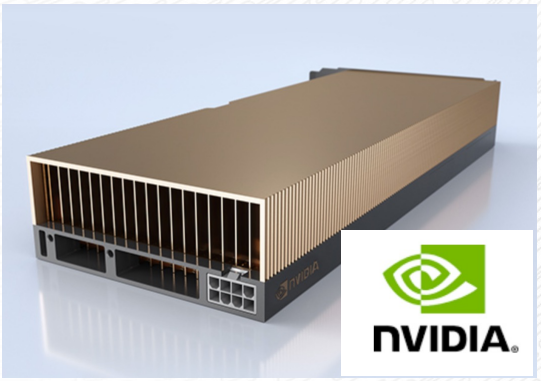
Manufacturing Has Been Trailblazing:

Curvy Designs (Wafer Targets) can be Manufactured Now

Multi-beam Mask Writer



Curvy ILT

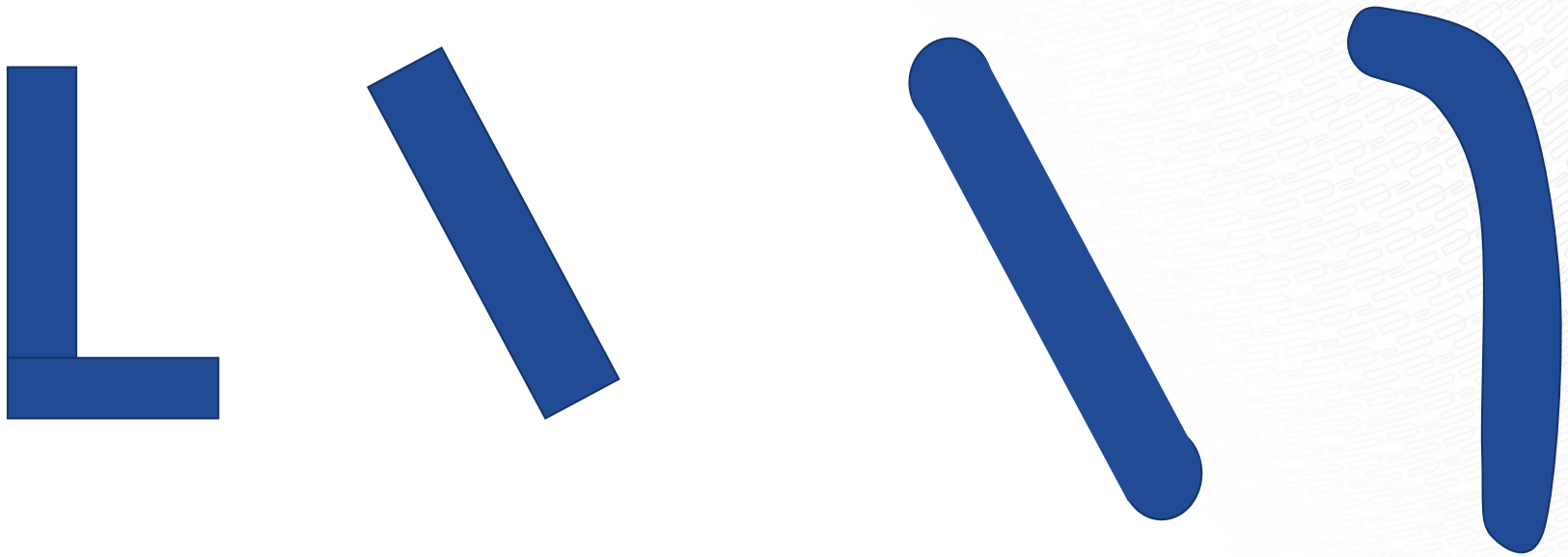


GPU Acceleration

Curvy Masks

“Curvy Design” Means Curvy Connections

Mask Shapes are All Curvilinear



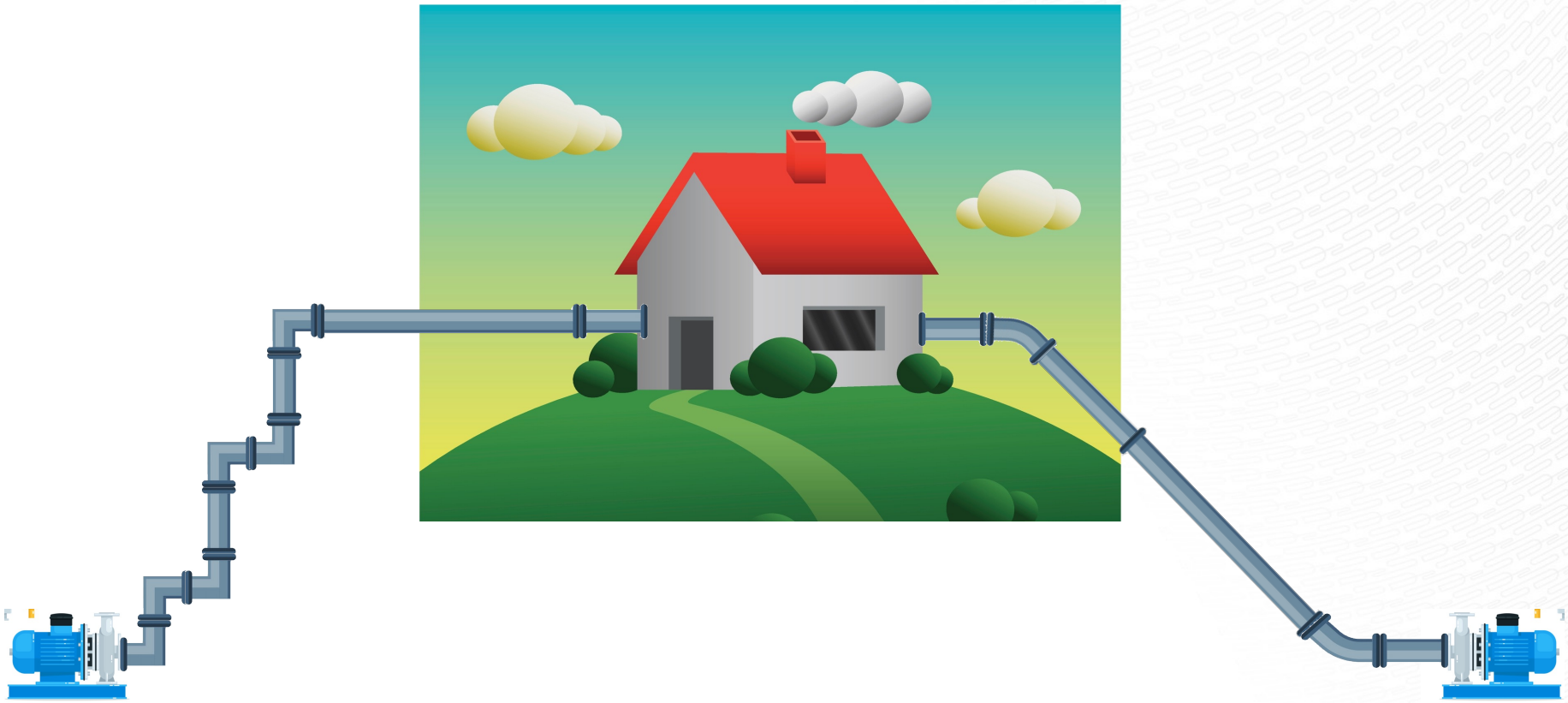
Manhattan Design

Non-Manhattan Design

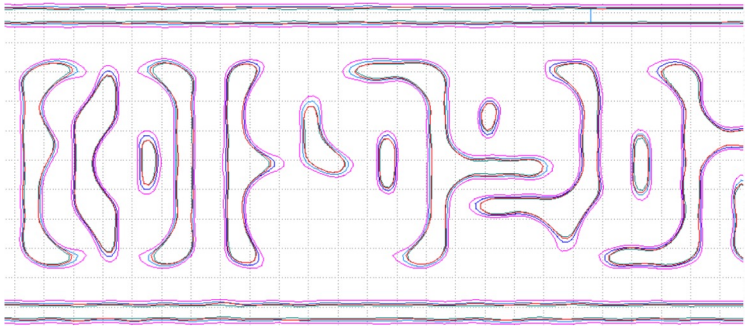
Curvy Design

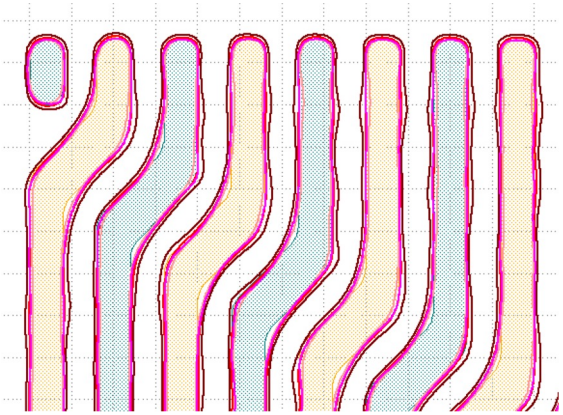
Curvy Design

Intuitively, the Efficiency of Curves Makes Sense

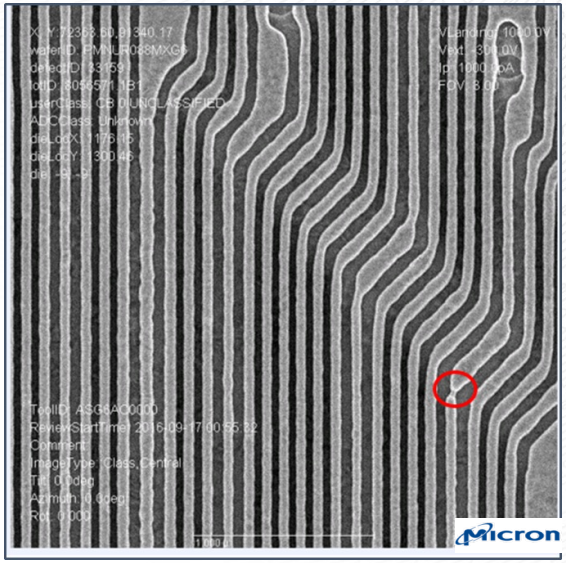


Curvy Design is Manufacturing-Aware Design





- Knowing what will be manufactured
  - Removes complex design rules
  - Tightens process corners with per-instance parasitic bounds
- Manufacturing target is achievable
- Curvy design is more reliably manufacturable
- Gains in
  - Performance
  - Power
  - Area
  - Yield

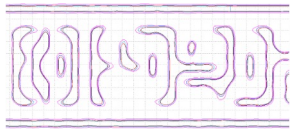


Could Curvy Routing Substantially Reduce Vias?

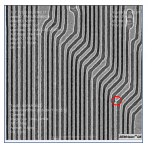
- High-rise buildings have nothing on the first floor but elevator shafts
- Chips have the same problem with vias
- Most chips are interconnect-limited
- Is it time to break the Manhattan assumption?

Four Things Needed to Enable Curvy Design

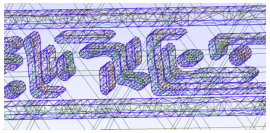
General Perception: "Everything has to Change"



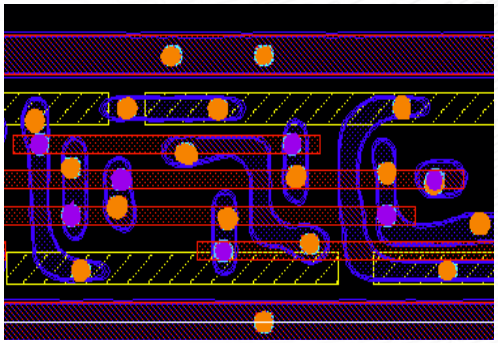
Custom Design

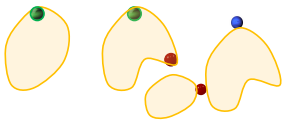


Routing



Parasitic Extraction





DRC

Imagine DAC 2025…

Engineering Track: Backend Design: **Early Results in Curvy Design**

1:30-1:45 “Routing without the Manhattan assumption”

1:45-2:00 “Custom layout for curvy shapes”

2:00-2:15 “Fast DRC of curvy designs”

2:15-2:30 “Capacitance extraction of curvy designs”

2:30-2:45 “Reducing power using curvy designs”

Future: Curvy Design Everywhere

Much Closer to "What You Design is What You Get"

Design

Manufacturing