JM3 Journal of Micro/Nanopatterning, Materials, and Metrology

RESEARCH PAPER

Make the impossible possible: use variable-shaped beam mask writers and curvilinear full-chip inverse lithography technology for 193i contacts/vias with mask-wafer co-optimization

Linyong (Leo) Pang,[a,*] Sha Lu,[a] Ezequiel Vidal Russell,[b] Yang Lu,[b] Michael Lee,[b] Jennefir Digaum,[b] Ming-Chuan Yang,[b] P. Jeffrey Ungar,[a] Michael Pomerantsev,[a] Mariusz Niewczas,[a] Kechang Wang,[a] Bo Su,[a] Michael Meyer,[a] and Aki Fujimura[a]

[a]D2S, Inc., San Jose, California, United States

[b]Micron Technology, Inc., Boise, Idaho, United States

ABSTRACT. Full-chip curvilinear inverse lithography technology (ILT) requires mask writers to write full reticle curvilinear mask patterns in a reasonable write time. We jointly study and present the benefits of a full-chip, curvilinear, stitchless ILT with mask-wafer co-optimization (MWCO) for variable-shaped beam (VSB) mask writers and validate its benefits on mask and wafer at Micron Technology. The full-chip ILT technology employed, first demonstrated in a paper presented at the 2019 SPIE Photomask Technology Conference, produces curvilinear ILT mask patterns without stitching errors, and with process windows enlarged by over 100% compared to the OPC process of record, while the mask was written by multibeam mask writer. At the 2020 SPIE Advanced Lithography Conference, a method was introduced in which MWCO is performed during ILT optimization. This approach enables curvilinear ILT for 193i masks to be written on VSB mask writers within a practical, 12-h time frame, while also producing the largest process windows. We first review MWCO technology, then curvilinear ILT mask patterns written by VSB mask writer, and then show the corresponding 193i process wafer prints. Evaluations of mask write times and mask quality in terms of critical dimension uniformity and process windows are also presented.

Keywords: curvilinear masks; photomask; GPU; inverse lithography technology; ILT; curvilinear ILT; mask wafer co-optimization; multibeam mask writer; variable-shaped beam mask writer; mask-data preparation

Paper 23056SS received Oct. 20, 2023; revised Dec. 5, 2023; accepted Dec. 14, 2023; published Feb. 6, 2024.

1 Introduction

1.1 Full-Chip, Curvilinear ILT is Now a Practical Reality

Inverse lithography technology (ILT)—a mathematically rigorous inverse approach that determines the mask shapes that will produce the desired on-wafer results—has been seen as a promising solution to many of the challenges of advanced-node lithography, whether optical or extreme ultraviolet (EUV). Since its introduction more than a decade ago,[1–17] there have been numerous studies that demonstrate that curvilinear ILT mask shapes, in particular, produce the

*Address all correspondence to Linyong (Leo) Pang, leo@design2silicon.com

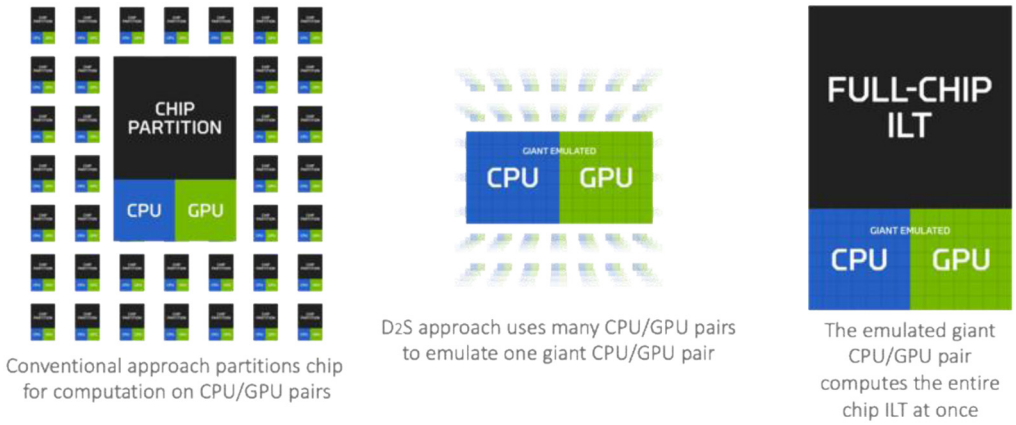


Fig. 1 TrueMask ILT, although comprising many GPU/CPU pairs, has been holistically designed so that it behaves as a single GPU/CPU pair, iterating on the entire chip as a whole, and avoiding stitching errors.

best process windows.[18] However, until recently, the runtimes associated with this computational technique have limited its practical application to critical "hotspots" on chips.[19] The solution to the runtime problem for ILT has been particularly vexing, as the traditional approach to runtime improvement—partitioning and stitching—has failed to produce satisfactory results, either in terms of runtime or in terms of quality. At the 2019 SPIE Photomask Technology Conference,[20] we detailed an entirely new, stitchless approach, creating a purpose-built system for ILT, called TrueMask® ILT. This system includes a unique graphics processing unit (GPU)-accelerated approach that emulates a single, giant GPU/CPU pair that can compute an entire full-chip ILT solution at once (Fig. 1). This approach, systematically designed for ILT and GPU acceleration, made full-chip ILT a practical reality in production for the first time.

The 2019 paper details how TrueMask ILT meets all of the requirements for a production-ready full-chip, curvilinear ILT solution: it integrates curvilinear mask rules to produce mask-rule-checking-clean results; it meets edge-placement error (EPE) requirements; its results are continuous and symmetric; it demonstrates both on-grid and off-grid invariance; and it is symmetric from any angle.

To validate TrueMask ILT results, D2S worked with Micron Technology to write masks and print wafers using the Micron Technology process of record (POR).[20,21] The ultimate goal for curvilinear ILT is to achieve the best process window, so in this evaluation, process windows were compared between OPC and TrueMask ILT using the Micron POR. Critical dimensions (CDs) were measured to quantify the size of the process window between OPC and TrueMask ILT.

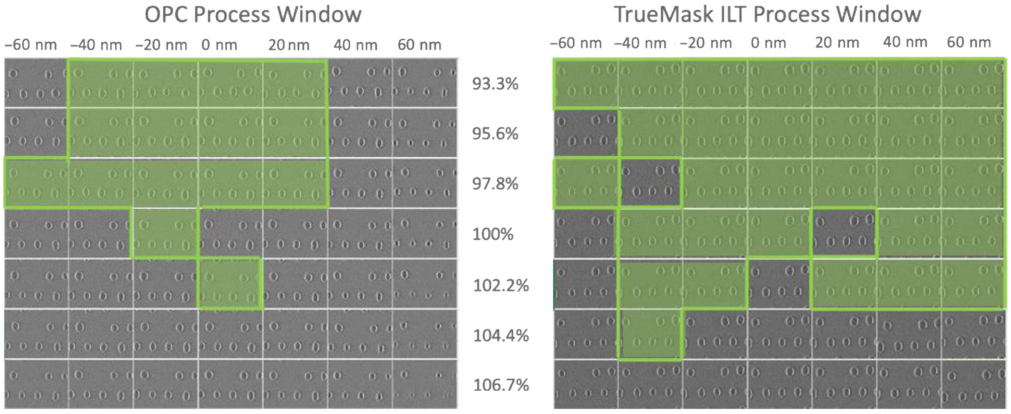


Fig. 2 Process window CD measurements for standard OPC versus TrueMask ILT of Micron Technology's POR. The green regions are within process window. Random contact target CD is 62.8 nm. 10% CD variation is used for process window criteria. TrueMask ILT increases the process window by more than 100%.[20]

Figure 2 shows the wafer-print matrix result for a random contact layer. These are all cases where the contacts are arranged in a Manhattan layout, without introducing nonorthogonal configurations. The target CD was 62.8 nm; all dies with CD within a 10% variation are considered to be within the required process window. The CD measurements that meet the conditions within the process window are highlighted in green in the chart. Note that the x axis is the focus, y axis is the dose (to be consistent with the process window plot). Three wafer images at the process center and two process corners are also shown below the charts. Compared to the Micron POR OPC, TrueMask ILT enlarged the process window by over 100%.

1.2 Could This Full-Chip Curvilinear ILT Approach Be Extended to VSB Mask Writing?

The approach detailed in the 2019 paper relied on multibeam mask writing, an important development in mask writing that is pixel-based, rather than shape-based, and so is shape-agnostic in terms of write time. The question that remained was if the benefits of full-chip, curvilinear ILT could be extended to the masks created by variable-shaped beam (VSB) mask writers that make up the majority of equipment in the mask shops around the world today. For 193i processing, advanced nodes need as much edge-placement accuracy as possible. The improved process windows that are possible from curvilinear ILT can help greatly. This is why it is important to enable curvilinear ILT for 193i to be written on widely available VSB mask writers.

In the 2020 paper, we detailed a mask-wafer co-optimization (MWCO) method that in combination with established techniques, such as overlapping shots and mask and wafer simulation, creates Manhattanized, full-chip, curvilinear ILT mask shapes that VSB mask writers can write within 12 h.[22] This paper will show the latest improvements and validate those results on real mask and wafer prints using VSB mask writing for 193i.

2 Mask-Wafer Co-optimization for Full-Chip Curvilinear ILT for VSB Mask Writers

2.1 Mask Data Preparation and Mask Process Correction for Curvilinear ILT Masks

The conventional approach to Manhattanizing curvilinear ILT masks requires a trade-off of accuracy for ILT runtime and the write time on the VSB mask writer. It is possible to get very close to a curvilinear target using many small rectilinear mask shapes to form curves with small "jogs" or "stair-steps." This approach creates fairly good curvilinear mask shapes using VSB writers. However, the shot count involved in this approach would lead to impractical write times if it were to be used on a full-chip ILT design. Alternatively, jog and step-sizes can be made larger, say 20 nm, to limit VSB shot count, but even then, if practiced at a full-chip scale, write times would be prohibitive using conventional fracturing (without overlapping shots). This practical reality, combined with the long runtimes of the traditional ILT software, even when running on a large bank of CPUs, has limited the use of ILT to small "hotspots." Yet the need to run ILT for hotspots suggests that there is general understanding that ILT produces superior process windows for the wafer.

2.2 Overlapping Shots and Simulation Enable Full-Chip, Curvilinear ILT Using VSB Mask Writers

The use of overlapping shots is a technique to reduce shots and improve dose margin for angled lines and curvilinear features to be written by VSB mask writers.[23,24] Figure 3 shows a typical curvilinear ILT mask pattern, fractured for a VSB mask writer. The pattern on the left uses conventional mask-data preparation (MDP) for VSB; the pattern on the right employs MDP with overlapping shots to create the same pattern. There are two observations from this example: first, overlapping shots can significantly reduce total shot count; and second, the majority of shots in this case (and in most production designs) are for the subresolution assist features (SRAFs)—which do not print—rather than for the main features. As we know, SRAFs have far less impact on the wafer EPE as compared to main features. For any given target main feature in a contact layer, an overwhelming number of shots are used for the SRAFs in a conventionally fractured solution. Overlapping shots produce SRAFs that perform well without devoting so much of the VSB write time to producing them.

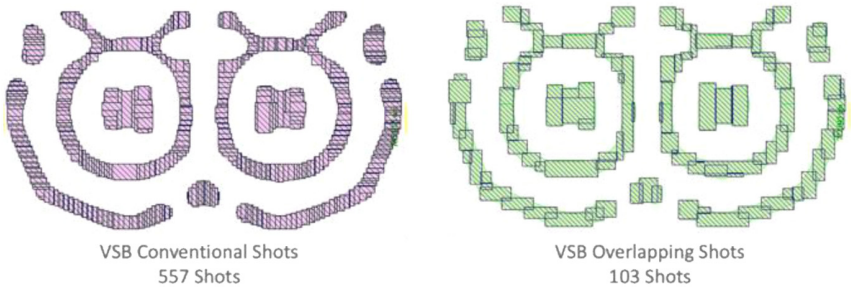


Fig. 3 Example of a curvilinear ILT mask pattern written by VSB mask writer with conventional (fracturing) shots and overlapping shots.

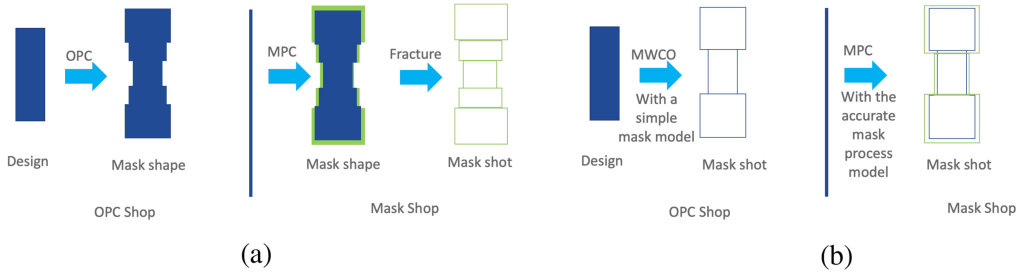
2.3 MWCO Shifts the OPC and Mask Shop Hand-off to Mask Shots

Today's semiconductor manufacturing process separates the responsibilities between the OPC/ILT shop and the mask shop [Fig. 4(a)]. The OPC/ILT shop has the responsibility to specify the desired mask shapes in order to achieve the best wafer results. They provide the post-OPC GDS/OASIS file specifying the mask shape. The mask shop has the responsibility to manufacture the masks as close as possible to the shapes specified by OPC/ILT. The mask shop takes the GDS/OASIS file containing the mask shape, runs mask process correction (MPC)—either rule-based or model based—then fractures the mask shape into rectangles, where each rectangle is a shot that VSB mask writer writes.

Realistic limitations of mask making are codified as mask design rules that the OPC/ILT shop needs to obey when specifying mask shapes. Other realities of mask making are considered in OPC/ILT as well, most notably the consideration that VSB mask writing is best for Manhattan (axis-parallel) rectangles with some provisions for 45-deg triangles. Since a major factor in mask cost and mask yield is mask write time, and the principle factor in mask write times (given a speed of resist dictated by the mask process for VSB-based mask writing) is the shot count, OPC/ILT tries to minimize mask shot count by various techniques, such as matching jog locations on opposite sides of a line.[25]

With ILT, a Manhattanization process is explicitly invoked wherein the wafer shape is optimized given a certain minimum jog size, such as 20 nm (mask dimensions), to avoid creating shapes that would take too many shots in the VSB writer.[26] But whether complex OPC or ILT, the specified mask shapes are complex, mostly rectilinear shapes with small 90-deg jogs, often with jog lengths of 20 nm (mask) or less. Manufactured with mask processes that have a blur radius of 20 to 25 nm (mask), these jogs are understood to become curves on the mask, often with the adjacent jogs interacting with each other. There is always a difference between the specified rectilinear shapes and the actual, curvilinear mask contours that result from that specification. Overlapping shots take advantage of this difference, using it as a tolerance in edge placement of the mask contour that can reduce shot count, while still shooting approximately the same contour, within the original EPE that the actual mask shape was going to have anyway.

In the traditional separation of responsibilities between the OPC shop and the mask shop, determining the overlapping shots that could write the mask shapes specified by the OPC shop



(a) (b)

Fig. 4 (a) Today, mask shape is the hand-off between OPC and mask shops. (b) MWCO shifts hand-off to mask shots.

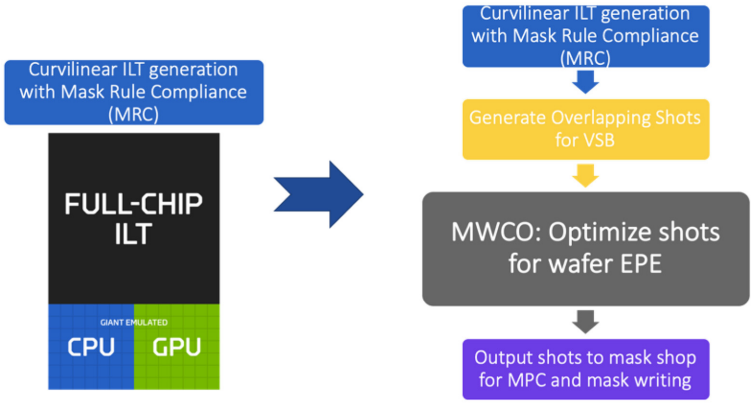


Fig. 5 MWCO flow for full-chip, curvilinear ILT for VSB mask writers.

was the domain of the mask shop. Even if error tolerances are within the original expectations, the idea that the originally specified shape is being slightly modified is disconcerting to the mask shop. Simulation-based contour checking is required; for example, because XOR checks will not pass.

MWCO marries curvilinear ILT with curvilinear MDP for VSB writers, using overlapping shots. MWCO incorporates overlapping shot generation and mask-wafer double simulation into the ILT process, so that the output of the OPC shop is already optimized for shot count (Fig. 5). Using double simulation, wafer EPE is iteratively optimized while manipulating VSB shot edges to produce rectilinear target mask shapes that are known to be writable on a VSB writer, with a known and an acceptable shot count. In the MWCO flow, the OPC shop hands off mask shots to the mask shop, instead of mask shapes [Fig. 4(b)]. The mask shop will still run MPC, with its more accurate mask process models, but the mask shop does not need to fracture the mask shape—the file given by the OPC shop is a shot list that VSB mask writer can write.

2.4 Actual Masks are Curvilinear: Even Rectilinear Mask Design Creates Curvilinear Masks

As discussed in the previous section, actual mask shapes are curvilinear, even when the specified shape is rectilinear [Fig. 6(a)].

Similar to lithography and wafer process, mask writing and mask process also are subject to proximity effects. In mask writing, a number of effects including beam blur and resist blur act as low-pass filters that rounds the shapes provided on input. In particular, highly jagged shapes with many 90 deg jogs that are 20 to 30 nm distance of each other will have much smoother curves than the input shapes suggest. Due to these effects, even when a designer and/or OPC engineer draw a rectilinear pattern, the result on mask will be a curvilinear mask pattern.

As shown in Fig. 6(b), the post-OPC/ILT contact main feature is a rectilinear pattern, while the simulation shows the mask pattern becomes a circular shape; the OPC/ILT design for the assist features is a rectilinear pattern with staircase jogs, while the simulation shows the mask patterns become smooth, curvy assist features on mask.

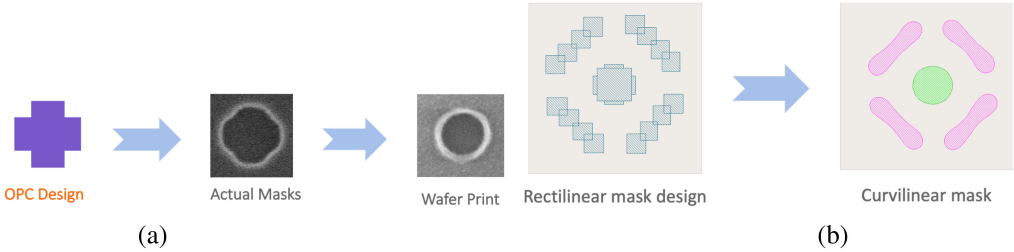


Fig. 6 (a) Example of OPC design, actual mask pattern (SEM image), and wafer pattern (SEM image). (b) Example of rectilinear mask design and its simulated curvilinear mask pattern.

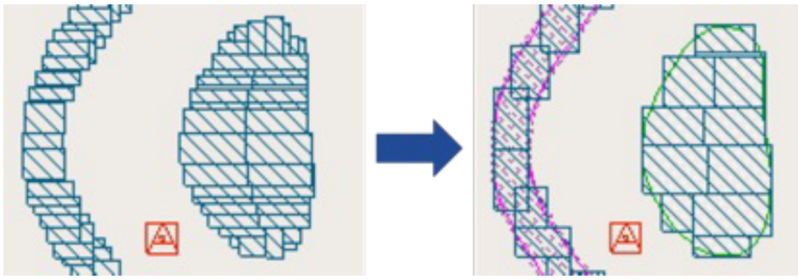


Fig. 7 Illustration of writing SRAFs with overlapping shots while writing main features with conventional shots.

2.5 Balance Shots for Write Time and Mask-Pattern Fidelity; Main Features: Conventional, SRAFs: Overlapping

The majority of the shot count for any given mask is from curvilinear SRAFs. In our case study (detailed in Sec. 3.2 of this paper) of a contact array with different densities, over 80% of the shots were needed to create the curvy SRAFs. Because SRAFs have relatively little impact on wafer EPE, overlapping shots can be used on SRAFs to dramatically reduce shot count. Main features, on the other hand, have a large impact on wafer EPE; therefore, conventional shots can be used for more precision, but still result in a much smaller number of shots than conventional fracture by leveraging eBeam and resist blur and accurate model-based mask simulation, as shown in Fig. 7.

2.6 MWCO: The Key is to Minimize and Move Shots based on Wafer EPE, not Mask EPE

Figure 8 shows an example contact array with curvilinear ILT producing desired curvilinear mask target shapes, then VSB shots being generated for it using overlapping shots as previously published.[23,24,27] In this figure, green lines show the wafer target, while red lines show the wafer image simulated from mask images simulated from the VSB shots in a double simulation process. The VSB shots are shown as hatched blue rectangles. Overlapping shots are used to shoot SRAFs on the mask that does not print on the wafer. For the SRAFs, thin brown lines reflect the target curvilinear mask shapes output by curvilinear ILT. Nonoverlapping shots shoot the main features, but with shot count just large enough to produce the target mask contour as specified by curvilinear ILT (not shown). MDP for overlapping shots is simulation-based, with iterative optimization to produce a shot configuration that produces the desired mask contour with a low shot count, taking advantage of the natural corner-rounding in the mask process, which is especially prominent with SRAF dimensions. To the right is a zoomed-in picture of the two main features on the lower right of the contact array. Without using MWCO, the red contour of the simulated wafer image comes within 2 nm EPE after mask-wafer double simulation. Because this process first produces the target curvilinear mask shapes using curvilinear ILT, and then separately optimizes the VSB shots to hit the desired mask contours, the trade-off with shot count inevitably results in accuracy loss, such as this 2 nm EPE.

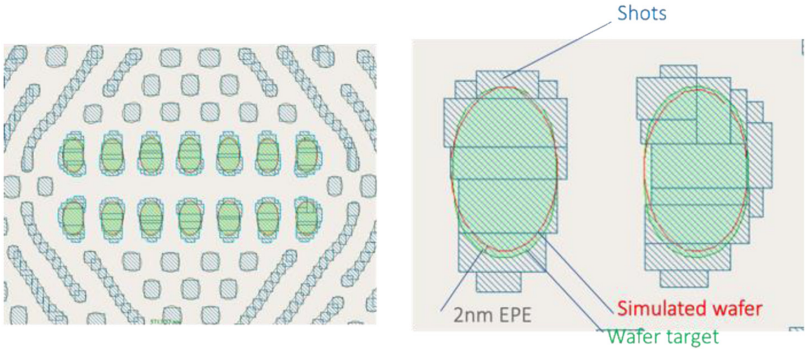


Fig. 8 VSB shots generated to minimize mask EPE.

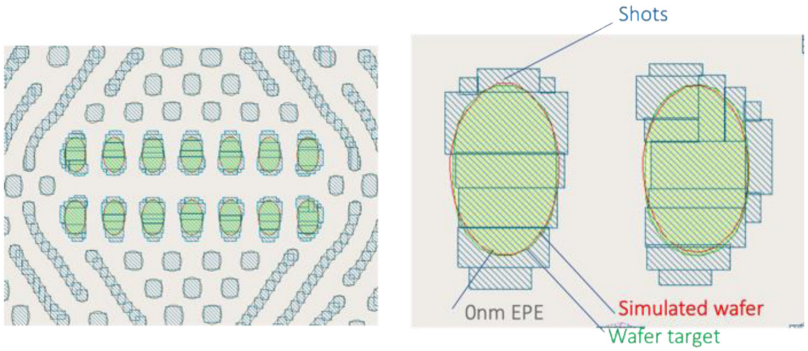


Fig. 9 VSB shots generated to minimize wafer EPE.

The wafer results can be much improved with MWCO. Figure 9 shows the results when the shots to produce the mask contours are moved based on mask-wafer double-simulated "wafer" EPE. By taking this approach, without changing the shot count or shot configuration much, the wafer EPE is reduced from 2 to 0 nm at the same location and <1 nm in all the shapes. Iteratively optimizing VSB shot edges while optimizing for wafer EPE significantly improves the ability to target curvilinear mask shapes while minimizing impact on shot count.

3 VSB Mask Write and Wafer Print Results for Full-Chip, Curvilinear ILT Using MWCO for 193i

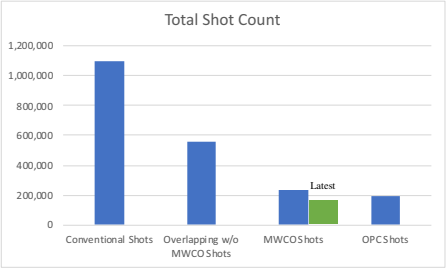
3.1 Targeting Wafer, not Mask, MWCO Produces ILT with VSB Shot Counts Comparable to OPC Designs

Once the optimization target is changed from mask to wafer, MWCO can further reduce the shot count, since the scanner is a band-limited optical system that will filter out high-frequency features on mask. Figure 10 shows three clips for the contact array sequence that was used in our 2019 paper.[20] It has 121 different configurations of a 11×11 contact array, each with slightly varied pitch and rotation angle. The contact array sequence includes features in a spectrum of placements, from dense placement to nearly isolated features, with the contact array rotated to demonstrate the underlying curvilinear, all-angle, nature of this solution. The total shot count when using conventional fracturing is a little over 1 million shots. Overlapping shots without MWCO reduces the shot count by roughly half to a little over half a million shots. MWCO reduces the shot count by half again, to a little less than a quarter million. The most recent MWCO result (not used in this tape-out) reduced the shots even further to <170 k shots. The OPC shot count is about 200k, so the MWCO shot count is comparable to or even less than OPC shot count, meaning the MWCO mask has about the same or less write time as OPC mask.

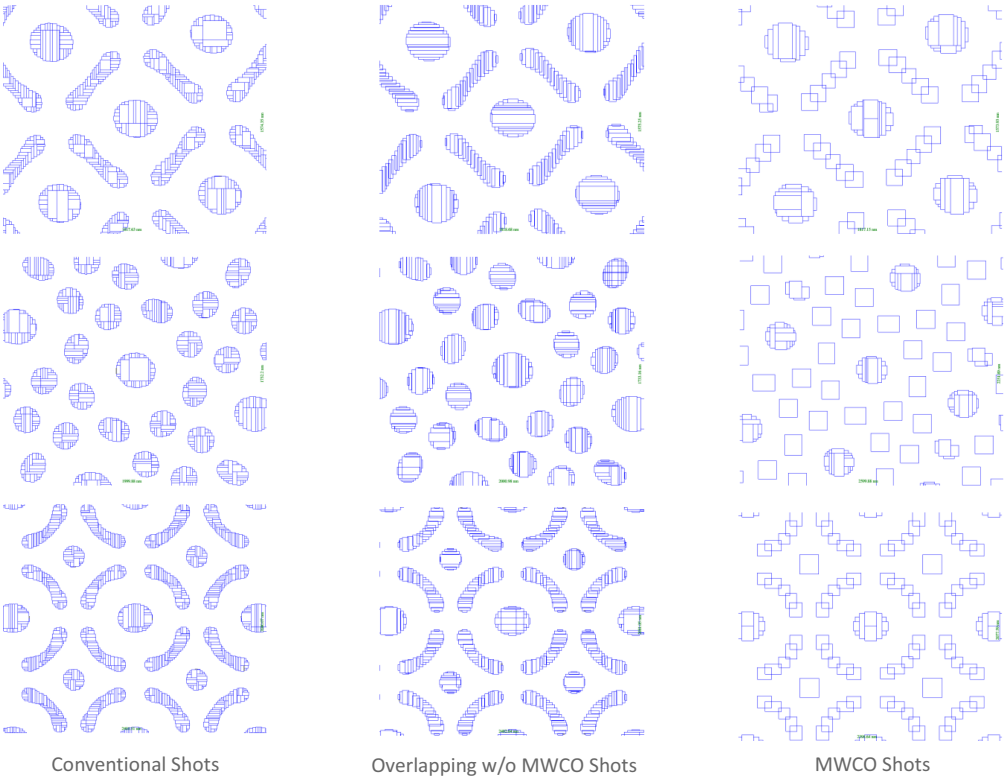
The actual mask was written by Micron mask shop using the NuFlare VSB mask writer EBM-9500 PLUS. Figure 11 shows mask SEM images for the three configurations from Fig. 10. One can see that the curvilinear ILT mask patterns were actually produced by the VSB mask writer. The curvilinear SRAFs in the MWCO do have staircase jogs, but since these SRAFs were made with large size overlapping shots, their dose margin is good.

3.2 MWCO Enables Even a VSB Mask Writer to Write Full-Chip, Curvilinear ILT Masks in 12 h

Previous works have shown that a multibeam mask writer[28] can write a full-chip, curvilinear ILT mask in 12 h for 193i processes.[20] The next question was, can a VSB mask writer write full-chip, curvilinear ILT masks for 193i within this same time frame? Figure 12 shows a write-time comparison chart presented by NuFlare, comparing write times between their VSB writer and their multibeam machine.[29] Because VSB mask write time is proportional to the number of shots, according to this NuFlare chart, it is only when shot count is >200 Gshots/pass that VSB write times exceed 12 h. Below the 200 Gshots/pass level, VSB write times are faster than 12 h even at 75 $\mu C/cm^2$. When this number is converted into shot density per square micron, it turns out the



(a)



(b)

Fig. 10 (a) VSB shot count and (b) shot configurations for three contact arrays. Note the POR OPC shot configurations are not shown in (b).

magic number is 36shots/μm^2. If the shot density is below this number, the mask write time using a VSB mask writer (i.e., NuFlare EBM 9500) will be <12 h.

MWCO was applied to the same contact array sequence used in the 2019 paper.[20] We applied MWCO to each pattern in the sequence to generate an overlapping VSB shot solution for each pattern. Figure 13 shows some examples in this sequence.

VSB shot density for each configuration in this array sequence is computed and shown in Fig. 14. Since this array sequence includes different sizes and rotations, effective areas that cover only the actual array region are used in the calculation. In other words, the empty area outside of the array is not used in the shot density calculation and therefore does not bias the shot density. The chart shows that the shot density for every configuration is below 36 shots/μm^2. There are three general regions in this sequence. The first region is dominated by main features. In this region, using bigger jogs/shots by using mask-wafer double-simulation is the magic behind the shot-count reduction. The second region is dominated by SRAFs. In this region, using overlapping shots on SRAFs dramatically reduces the shot count to keep shot density below 36 shots/μm^2. The third region is still dominated by SRAFs, but due to a larger pitch, the pattern density is lower, making the shot density even lower than the first or second regions—well below

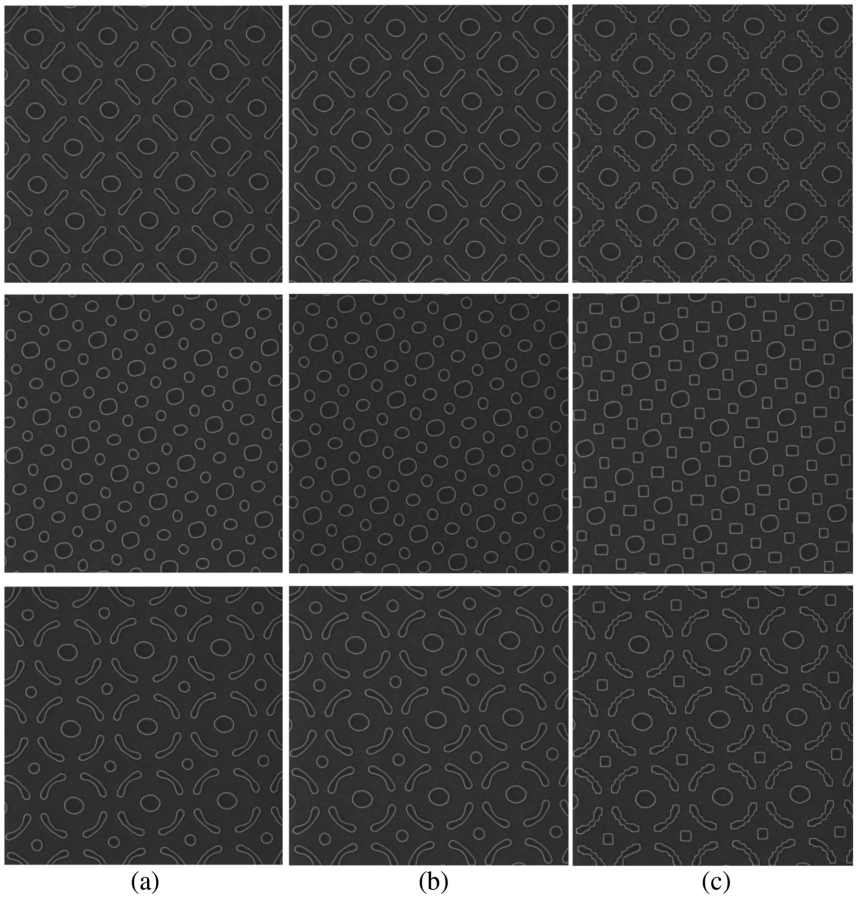


Fig. 11 Mask SEM images of VSB shot for three contact arrays with (a) conventional shots, (b) overlapping without MWCO, and (c) MWCO.

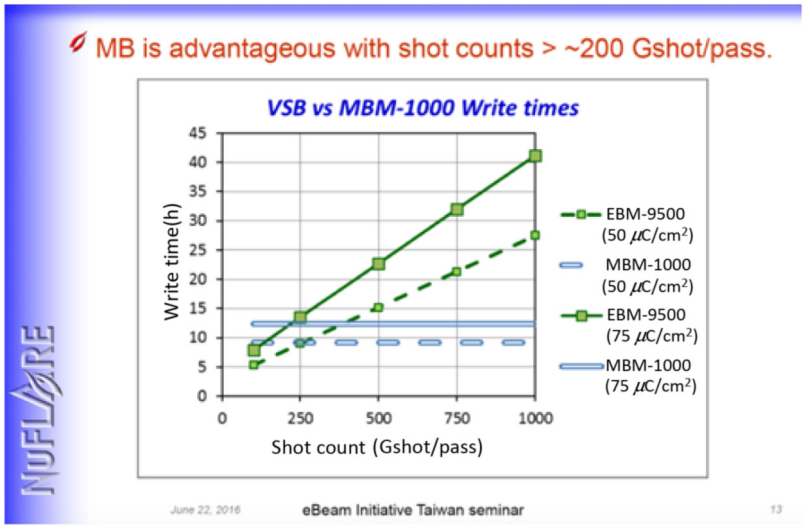


Fig. 12 NuFlare's estimation of mask write time for their VSB mask writer and multibeam mask writer.[28]

36 shots/μm^2. The chart also shows that using conventional shots (the red line) results in shot densities that are much higher, with minimum about 180 shots/μm^2, which translates to about 5× the write time. For the second region, due to curvilinear SRAFs, the write time for conventional shots skyrockets, to 10×.

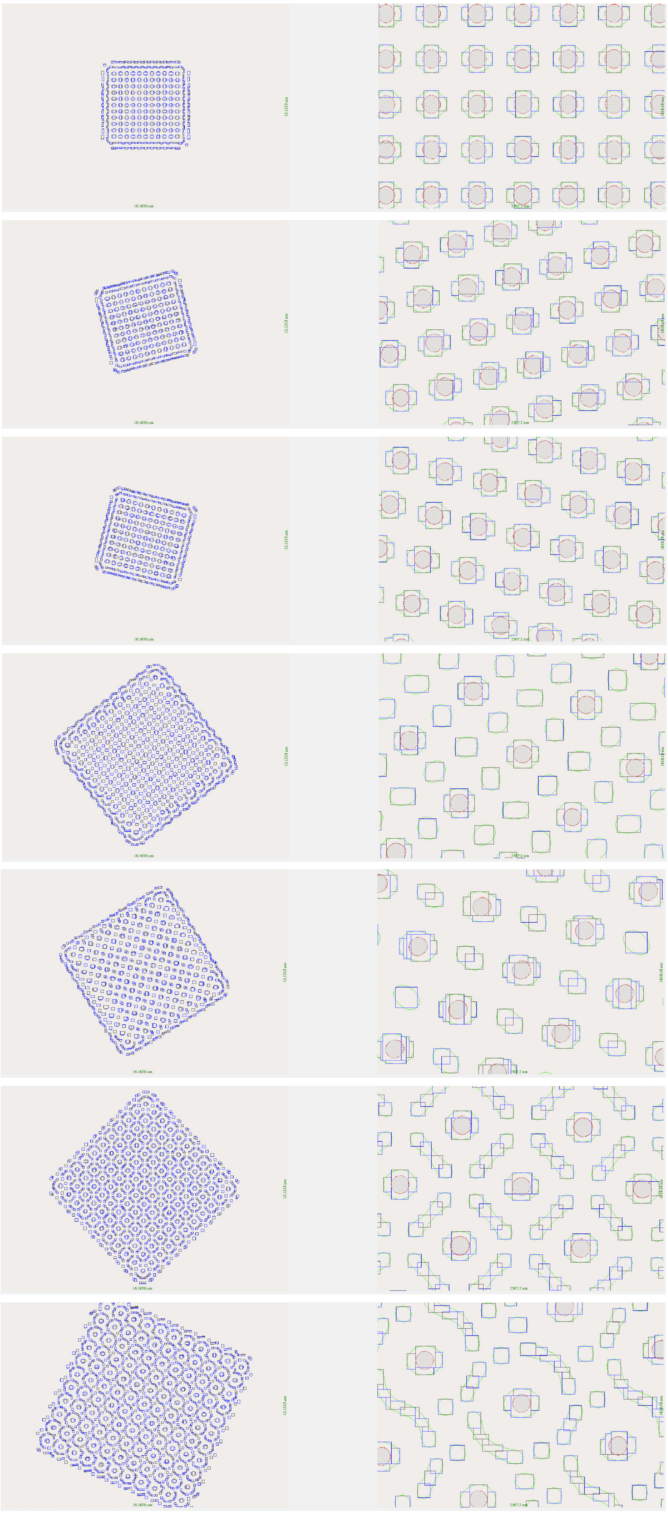


Fig. 13 MWCO results for contact array sequence from 2019 paper.

3.3 Curvilinear ILT Mask and Corresponding Wafer Results Using MWCO

Figure 15 shows SEM images of curvilinear ILT mask and its corresponding wafer print for the same contact array used in previous sections. The contact ADI target is 40 nm, and the minimum pitch is 100 nm. One can see that the contact array was printed nicely with this MWCO curvilinear ILT mask: the contact holes are printed evenly across all the varied pitches and rotations,

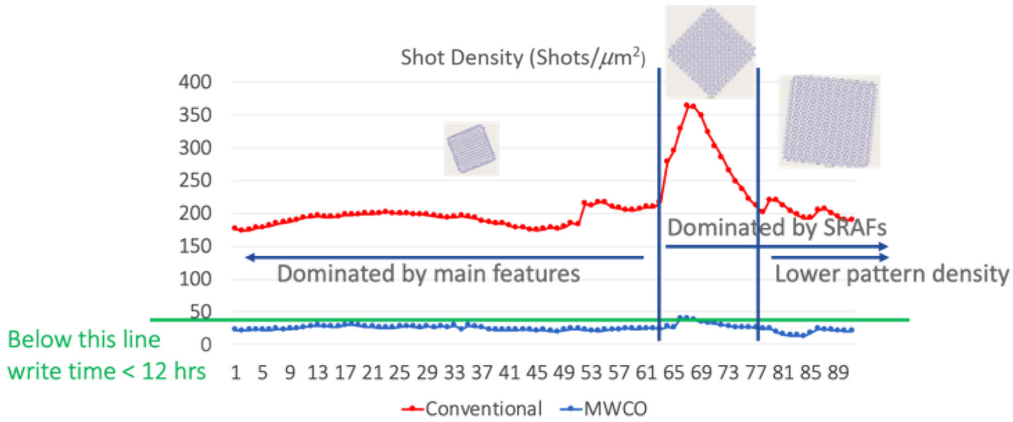


Fig. 14 VSB shot density of MWCO results for the contact array sequence from Fig. 11.

as well as from the center of the array all the way to the edge of the array, which is very challenging for OPC.

3.4 MWCO Produces 2× Larger Process Windows than OPC

The 2019 paper demonstrated that curvilinear ILT (in that case, written with a multibeam mask writer) produces the largest process window. We have already seen that MWCO reduces the shot count and mask write time by 4× on VSB mask writer, as compared to conventional shots. Does ILT with MWCO written by a VSB writer produce similar process window enlargement benefits?

For this study, 61 different patterns—including some of the most challenging ones found in lithography and OPC—were selected. They were treated with conventional OPC VSB shots, curvilinear ILT using overlapping VSB shots without MWCO, and overlapping VSB shots with MWCO. All of the patterns were written on the same mask using the NuFlare VSB mask writer EBM-9500 PLUS. The wafer was printed at seven different focuses and nine doses, for a total of 63 different process conditions (Fig. 16).

Figure 17 shows the distribution of mean-to-target value for all measurement sites at the nominal condition. One can see the bias for conventional OPC, curvilinear ILT with overlapping shots without MWCO, and curvilinear ILT with overlapping shots with MWCO are all around −5 nm. The CD variation distributions for three cases are also about the same. This provides a fair comparison basis when we look at variations when process condition changes.

Figure 18 shows the CD variation distribution for all 63 process conditions. Instead of plotting mean-to-target as in Fig. 17, here maximum CD minus minimum CD for all process variations for each pattern and measurement site is used. That is why the numbers are all positive. It is very clear that curvilinear ILT using overlapping shots without MWCO and curvilinear ILT using overlapping shots with MWCO reduces the CD average variation by about 3×, from 20 to 7 nm. In addition, the CD variation spread is also narrowed by half.

Figure 19 shows the process window plot. The x axis is the focus, and the y axis is the dose change. Since there are 61 sites, we plot the ratio of the number of sites meeting the process window requirement to the total number of sites. A CD variation of 10% is used as the process window criteria. The pseudocolor from green to red represents process window from good to bad. Overall curvilinear ILT using overlapping shots without MWCO and curvilinear ILT using overlapping shots with MWCO greatly enlarged the green (or non-red) region by over 2×, especially the depth of focus. Comparing overlapping without MWCO and with MWCO, the MWCO is slightly better, showing the benefit of optimizing wafer EPE instead of mask EPE while only using half the number of shots as the overlapping shots without MWCO case.

4 Summary and Conclusions

4.1 ILT Vision Realized: Full-Chip Curvilinear ILT with Full Mask VSB Writing in 12 h for 193i

For more than a decade, the semiconductor industry has recognized the value of ILT in addressing the challenges of advanced-node lithography. Until now, runtime and VSB write times have

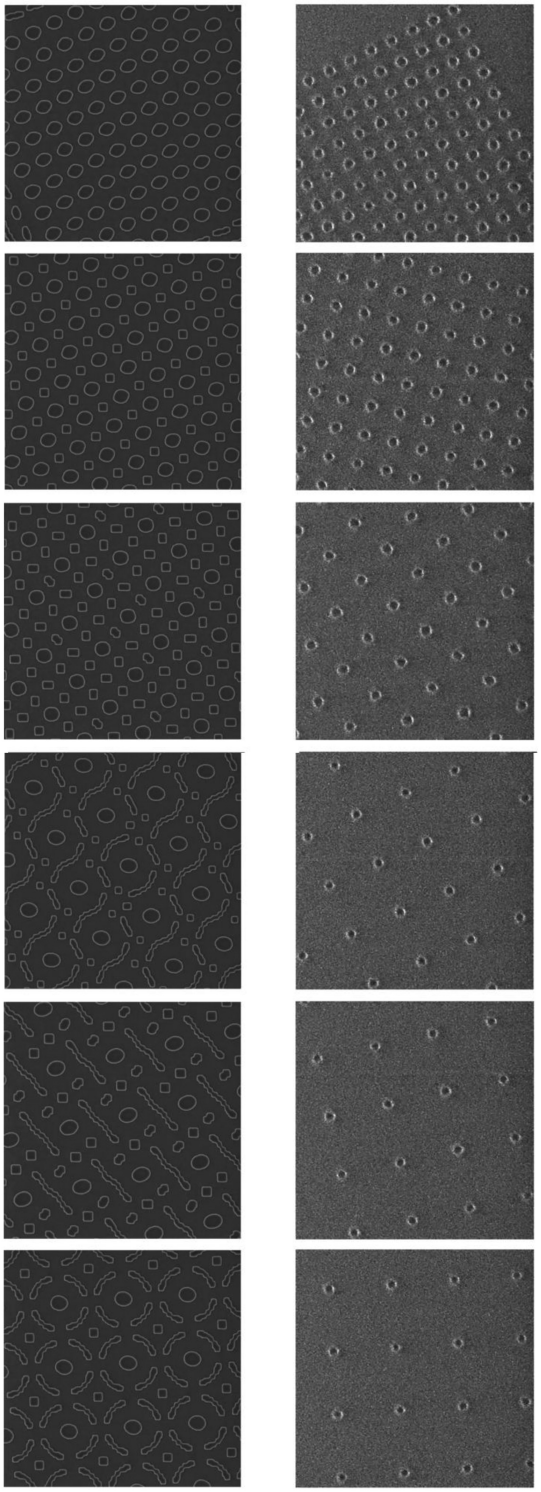


Fig. 15 MWCO results for the same contact array used in the 2019 paper. In each pair, (a) MWCO VSB mask SEM images of curvilinear mask designs for different pitches and orientations and (b) SEM images of corresponding wafer print.

been insurmountable barriers to using ILT as a full-chip solution. By embracing a unique, holistically conceived, purpose-built system of GPU-accelerated hardware and software that emulates a single giant GPU/CPU pair, stitchless, curvilinear, full-chip ILT is now a practical reality as demonstrated in the 2019 paper.

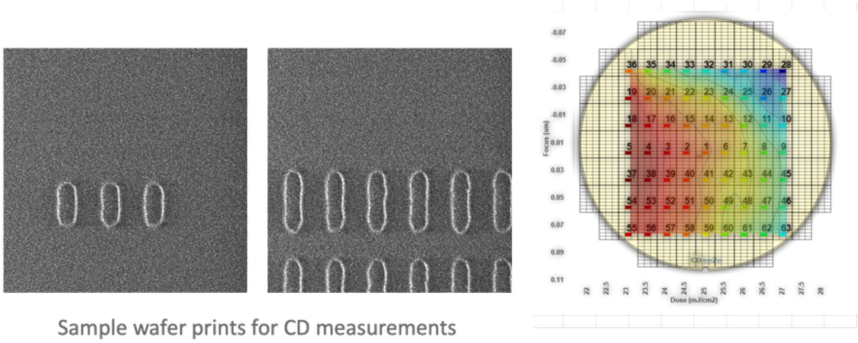


Fig. 16 Wafer process window study to compare curvilinear ILT produced with different VSB options and OPC.

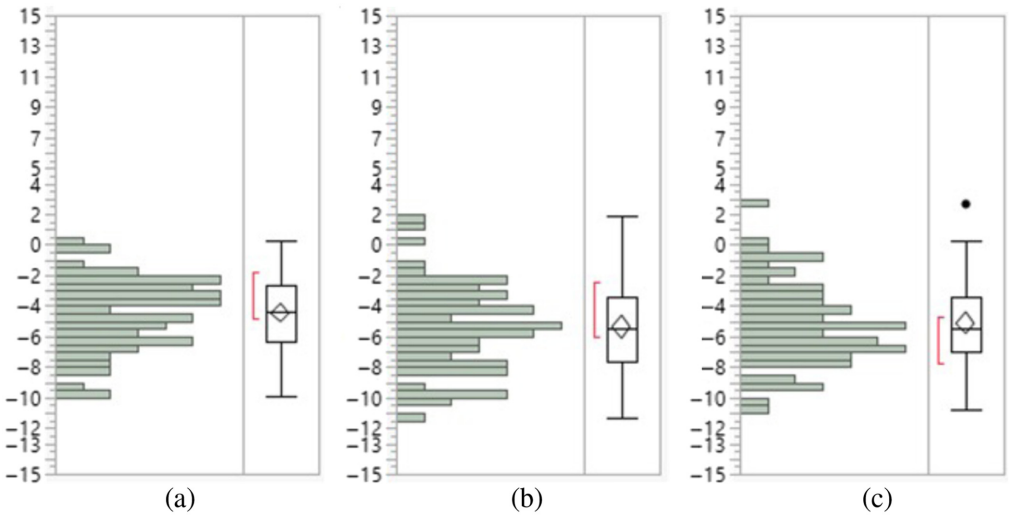


Fig. 17 CD mean-to-target variations for all 61 test patterns/site at the nominal condition for (a) OPC, (b) curvilinear ILT using overlapping shots without MWCO, and (c) MWCO.

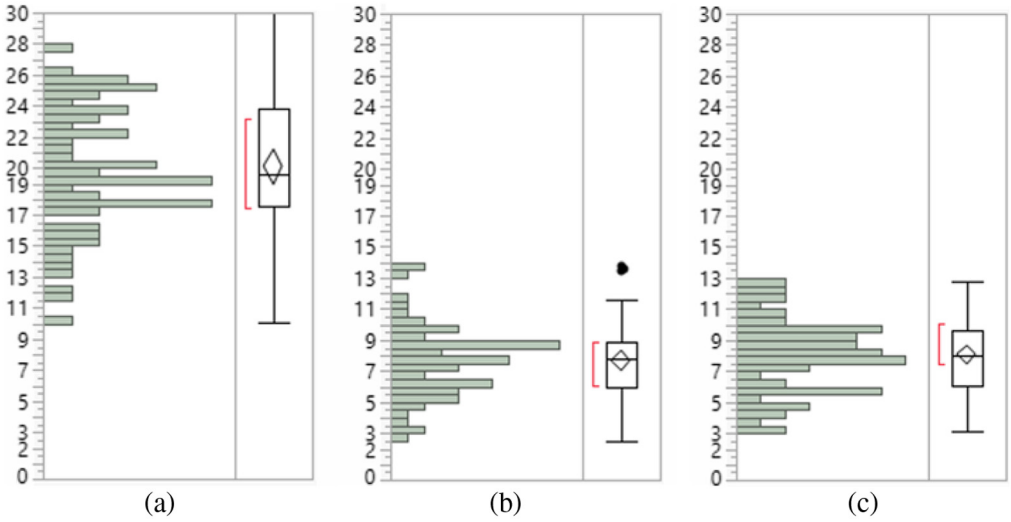


Fig. 18 CD maximum minus minimum variations within all 63 process conditions for all 61 test patterns/site for (a) OPC, (b) curvilinear ILT using overlapping shots without MWCO, and (c) MWCO.

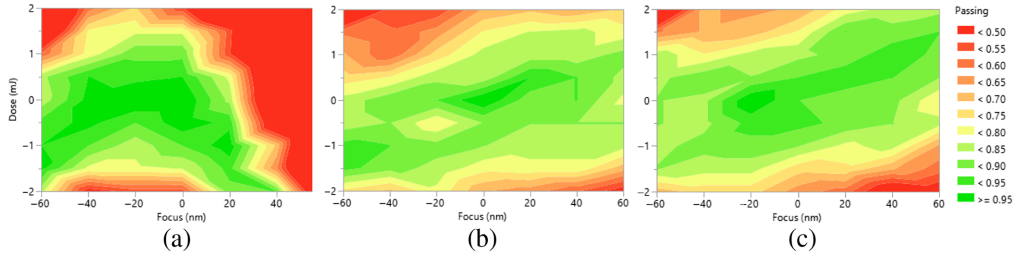


Fig. 19 Process window plots for all 61 test patterns/sites at the all 63 process conditions for (a) OPC, (b) curvilinear ILT with overlapping shots without MWCO, and (c) curvilinear ILT using overlapping shots with MWCO.

MWCO is now introduced as a further enhancement, combining overlapping shots with mask and wafer double-simulation to demonstrate that curvilinear ILT for 193i is practical with VSB mask writers. Extensive mask and wafer experiments were performed to study curvilinear ILT using conventional shots, overlapping shots without MWCO, overlapping shots with MWCO, and OPC to produce patterns commonly seen in memory applications. Tens of thousands of mask and wafer SEM images and CD measurements were collected and analyzed. The mask data showed overlapping shots without MWCO and with MWCO can enable a VSB mask writer to produce accurate curvilinear ILT masks. The mask write time using overlapping shots with MWCO is even less than conventional OPC. The wafer results for both curvilinear ILT using overlapping shots without MWCO and with MWCO reduced CD variation by 3× over OPC at all process variations, and enlarged the process window by 2× over conventional OPC. MWCO has slightly better process window than overlapping without MWCO but with only half of the shot count or mask write time. These results demonstrate that by employing MWCO, VSB writers can write a curvilinear ILT mask within 36 shots/μm^2, which, for resist sensitivities expected for 193i masks, should be below 12 h in write time. MWCO becomes an enabler for non-EUV leading edge to keep improving their lithography process and yield and also will enable curvilinear designs in the future. It completes the last piece of the full-chip curvilinear ILT puzzle, making it available for all technology nodes and all mask shops.

Disclosures

Company proprietary information will not be made available, but manuscript content is consistent with JM3 technical content guidelines.

Code and Data Availability

The data presented in this paper are not available as it constitutes preparatory data.

Acknowledgments

This work was funded by the institutes for which the authors work. Furthermore, this paper has been revised and updated based on our previous SPIE Proceedings paper presented at SPIE Photomask Technology 2020.[30,31]

References

1. B. E. A. Saleh and S. I. Sayegh, "Reductions of errors of microphotographic reproductions by optical corrections of original masks," *Opt. Eng.* **20**, 781–784 (1981).
2. K. M. Nashold and B. E. A. Saleh, "Image construction through diffraction-limited high-contrast imaging systems: an iterative approach," *J. Opt. Soc. Am. A* **2**, 635 (1985).
3. Y. Liu and A. Zachor, "Optimal binary image design for optical lithography," *Proc. SPIE* **1264**, 410–412 (1990).
4. Y. Liu and A. Zachor, "Binary and phase-shifting image design for optical lithography," *Proc. SPIE* **1463**, 382–399 (1991).
5. A. Rosenbluth et al., "Optimum mask and source patterns to print a given shape," *J. Microlith., Microfab., Microsyst.,* **1**, 13–30 (2002).

6. Y.-T. Wang et al., "Automated design of halftoned double-exposure phase-shifting masks," *Proc. SPIE* **2440**, 290–301 (1995).
7. Y. H. Oh and J.-C. Lee, "Resolution enhancement through optical proximity correction and stepper parameter optimization for 0.12-μm mask pattern," *Proc. SPIE* **3679**, 607–613 (1999).
8. T. Fuhner and A. Erdmann, "Improved mask and source representations for automatic optimization of lithographic process conditions using a genetic algorithm," *Proc. SPIE* **5754**, 415–426 (2005).
9. D. S. Abrams and L. Pang, "Fast inverse lithography technology," *Proc. SPIE* **6154**, 61541J (2006).
10. L. Pang, Y. Liu, and D. Abrams, "Inverse lithography technology (ILT): what is the impact to the photomask industry?" *Proc. SPIE* **6283**, 62830X (2006).
11. Y. Liu et al., "Inverse lithography technology principles in practice: unintuitive patterns," *Proc. SPIE* **5992**, 599231 (2005).
12. B. Lin et al., "Inverse lithography technology at chip scale," *Proc. SPIE* **6154**, 615414 (2006).
13. C.-Y. Hung et al., "Pushing the lithography limit: applying inverse lithography technology (ILT) at the 65 nm generation," *Proc. SPIE* **6154**, 61541M (2006).
14. J. Ho et al., "Real-world impacts of inverse lithography technology," *Proc. SPIE* **5992**, 59921Z (2005).
15. A. Moore et al., "Inverse lithography technology at low k1: placement and accuracy of assist features," *Proc. SPIE* **6349**, 63494T (2006).
16. C.-Y. Hung et al., "First 65 nm tape-out using inverse lithography technology (ILT)," *Proc. SPIE* **5992**, 59921U (2005).
17. C.-W. Chu et al., "Enhancing DRAM printing process window by using inverse lithography technology (ILT)," *Proc. SPIE* **6154**, 61543O (2006).
18. B.-G. Kim et al., "Trade-off between inverse lithography mask complexity and lithographic performance," *Proc. SPIE* **7379**, 73791M (2009).
19. "2018 eBeam initiative perceptions survey results," (18 September 2018). http://www.ebeam.org
20. L. Pang et al., "Study of mask and wafer co-design that utilizes a new extreme SIMD approach to computing in memory manufacturing: full-chip curvilinear ILT in a day," *Proc. SPIE* **11148**, 111480U (2019).
21. E. Russell, "ILT and curvilinear mask designs for advanced memory designs," presented at SPIE eBeam lunch (25 February 2020). http://www.ebeam.org
22. L. L. Pang et al., "TrueMask ILT MWCO: full-chip curvilinear ILT in a day and full mask multi-beam and VSB writing in 12 hrs for 193i," *Proc. SPIE* **11327**, 113270K (2020).
23. A. Fujimura et al., "Best depth of focus on 22-nm logic wafers with less shot count," *Proc. SPIE* **7748**, 77480V (2010).
24. H. Zable et al., "Writing wavy metal 1 shapes on 22-nm logic wafers with less shot count," *Proc. SPIE* **7748**, 77480X (2010).
25. L. Pang et al., "Inverse lithography technology (ILT): keep the balance between SRAF and MRC at 45 and 32 nm," *Proc. SPIE* **6730**, 673052 (2007).
26. L. Pang et al., "Laser and e-beam mask-to-silicon with inverse lithography technology," *Proc. SPIE* **5992**, 599221 (2005).
27. L. Pang et al., "Model-based MPC enables curvilinear ILT using either VSB or multi-beam mask writers," *Proc. SPIE* **10454**, 1045407 (2017).
28. C. Klein and E. Platzgummer, "MBMW-101: world's 1st high-throughput multi-beam mask writer," *Proc. SPIE* **9985**, 998505 (2016).
29. H. Matsumoto et al., "Multi-beam mask writer MBM-1000 and its application field," *Proc. SPIE* **9984**, 998405 (2016).
30. L. L. Pang et al., "Enabling faster VSB writing of 193i curvilinear ILT masks that improve wafer process windows for advanced memory applications," *Proc. SPIE* **11518**, 115180W (2020).
31. L. Pang, "Inverse lithography technology: 30 years from concept to practical, full-chip reality," *J. Micro/Nanopattern. Mater. Metrol.* **20**(3), 030901 (2021).

Linyong (Leo) Pang has been the chief product officer and executive VP at D2S since 2014, leading the TrueMask mask data preparation products and the new generation full chip curvilinear inverse lithography technology products using GPU acceleration. Prior to D2S, he was the Sr. Vice President of Computational Lithography and Inspection Technologies at Luminescent Technologies. He joined the luminescent executive team from its beginning in 2004 and pioneered the development of ILT products (Acquired by Synopsys in 2012) and, later on, Computational Metrology and Inspection business until it was acquired by KLA-Tencor in March 2014. His pioneering work in EDA and semiconductors started back 1999 at Numerical Technologies as the inventor and product manager of the i-Virtual Stepper System. He has 38 issued patents, 27 pending patents, and 85 publications. He was recognized as a SPIE fellow

in 2023. He received his MS degree in computer science and his PhD in mechanical engineering from Stanford University.

Sha Lu has more than 25 years of experience in EDA physical design software development. She was the first to use nonlinear programming to solve global placement problems, taking into account topological and physical requirements at the same time. Currently, she is solving challenging problems related to mask generation. She received her PhD in electrical engineering from Stanford University.

Ezequiel Vidal Russell is the senior director of Mask Technology at Micron Technology. He joined Micron in 2002 in research and development working on photolithography masks for the manufacturing of microchips, with emphasis on resolution enhancement techniques and optical proximity corrections. He earned a licenciado diploma degree in physics in 1996 and his PhD in physics in 2001 both from the Instituto Balseiro, Bariloche, Argentina.

Yang Lu is a principle central mask engineer at Micron Technology working on mask design and mask data preparation. Prior to his current position, he was a senior tapeout CAD engineer and R&D lithography engineer at Micron Technology. He received his MS degree in computer science and electrical engineering from Michigan State University.

Michael Lee is a senior member of the technical staff—AMD RTD at Micron Technology. He is currently working in the Advanced Mask Development Group on OPC recipe development. He has worked at the Semi-Conductor Industry for more than 38 years in areas spanning design, fab process, reliability, metrology, final test, OPC, database design, AI systems, and various software development projects. His degree is in mathematics with emphasis in scientific computing.

Jennefir Digaum received his PhD in optics and photonics from the College of Optics and Photonics at the University of Central Florida in 2016. He joined Micron in 2016 as an RET design engineer for 3DNAND. Currently, he is the RET design lead engineer supporting both DRAM and emerging memory in Micron's Advanced Mask Development Group. He is a regular member of SPIE and has (co-)authored peer-reviewed journals, conference proceedings, and a book chapter.

Ming-Chuan Yang received his PhD in electrical and computer engineering from Purdue University, West Lafayette, Indiana, United States. He joined Micron Technology in 2007 with focus on resolution enhancement techniques and is now a senior member of technical staff, leading Micron RET/OPC Group supporting leading-edge semiconductor memory technologies. Before 2007, he was responsible for photolithography simulation tools and computational lithography techniques for Intel Corporation.

P. Jeffrey Ungar received his PhD in physics from Stanford University and his BSc degree in engineering physics from Queen's University. He is currently a chief scientist for TrueMask ILT at D2S, Inc. He has more than 40 issued patents in many technologies, including computer graphics, power conversion circuitry, lithium ion batteries, and ILT algorithms.

Michael Pomerantsev has been a senior member of Consulting Staff at D2S, Inc. since 2013. He graduated from UCLA with his MS in computer science and his PhD in mathematics. Since then he worked at several EDA companies and CAD departments. His mathematical curiosity includes topology, especially knot theory, and algorithms, especially geometric ones. His professional interests include physical design automation, inverse lithography, and fast scalable algorithms.

Mariusz Niewczas is currently a senior member of Consulting Staff at D2S Inc. Previously, he worked at AboundLogic and PDF Solutions Inc. He holds his PhD in EE and his MSc degree from Warsaw University of Technology, Poland, and has spent over 10 years as an academic teacher and researcher, first at Warsaw University of Technology and then at Carnegie Mellon University. He has published more than 40 papers and holds several patents.

Kechang Wang has been a senior application engineer at D2S for 8 years, and specializes in their products such asTrueMask MDP, TrueMask, and Inverse Lithography Technology (ILT). Previously, he worked 9 years in the same role at Luminescent, focusing on ILT customer

adoption, mask inspection, and defect management. His experience also includes a tenure at Synopsys, working on mask data preparation software, and at Photronics, where he automated processes for mask data preparation, inspection, and metrology.

Bo Su has been at D2S Inc. for nearly 10 years and currently as Sr. Product Management director. He has more than 28 years semiconductor IC industry working experiences and has more than 70 scientific and technical publications and co-authored a book, titled *Introduction to Metrology Applications in IC Manufacturing*. Since 2018, he has served as an associated editor of JM3. He has a PhD in physics.

Michael Meyer obtained his BS CS degree from UN-L and MS EE from CMU. He has worked at ATT Bell Labs, SDA, Cadence Design Systems, Sonics, and D2S in EDA, Silicon IP, and software for semiconductor manufacturing.

Aki Fujimura is the chairman and CEO of D2S, Inc. Previously, Aki served as CTO at Cadence Design Systems and President/COO/inside board member of Simplex Solutions. He was also an inside board member and VP at Pure Software. He was a founding member of Tangent Systems in 1984, which was acquired by Cadence Design Systems in 1989. He was recognized as a SPIE fellow in 2023. He received his BS/MS degrees in electrical engineering from MIT.