Aki Fujimura, CEO D2S, Inc.| August 22, 2025 for the SPIE BACUS Webinar Series

Ask for What You Can Get and Get What You Ask For

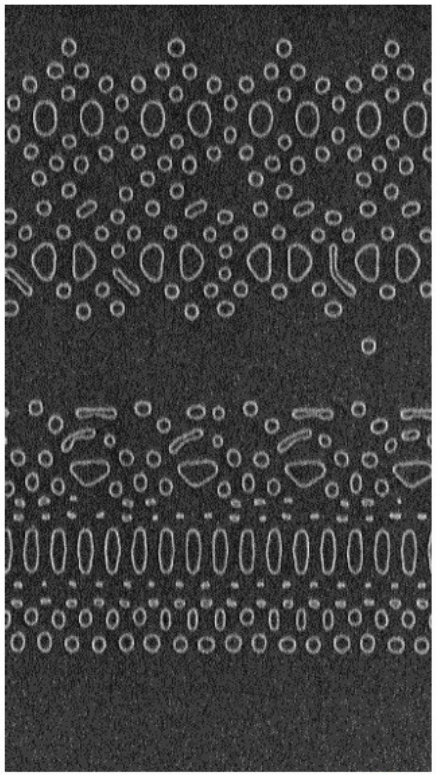
All manufacturable shapes are curvy

Ezequiel was Right…

Why Curvilinear Masks

- **More degrees of freedom for OPC solutions**
  - *Assist features:* improved process window, optimal placement
  - *Main features:* infinitesimally small segmentation of OPC, higher degree of control of the correction
  - Physically meaningful MRCs (no corner-to-corner)
  - Accurate target representation for Mask **and** Wafer
- **Mask Fidelity**
  - Improved matching between mask and intended OPC shapes
  - More accurate OPC models
    - No need to compensate for differences between "intended" shape and mask shape
  - Mask friendly shapes (no sharp corners)
    - Mask uniformity: reduces variations at feature corners

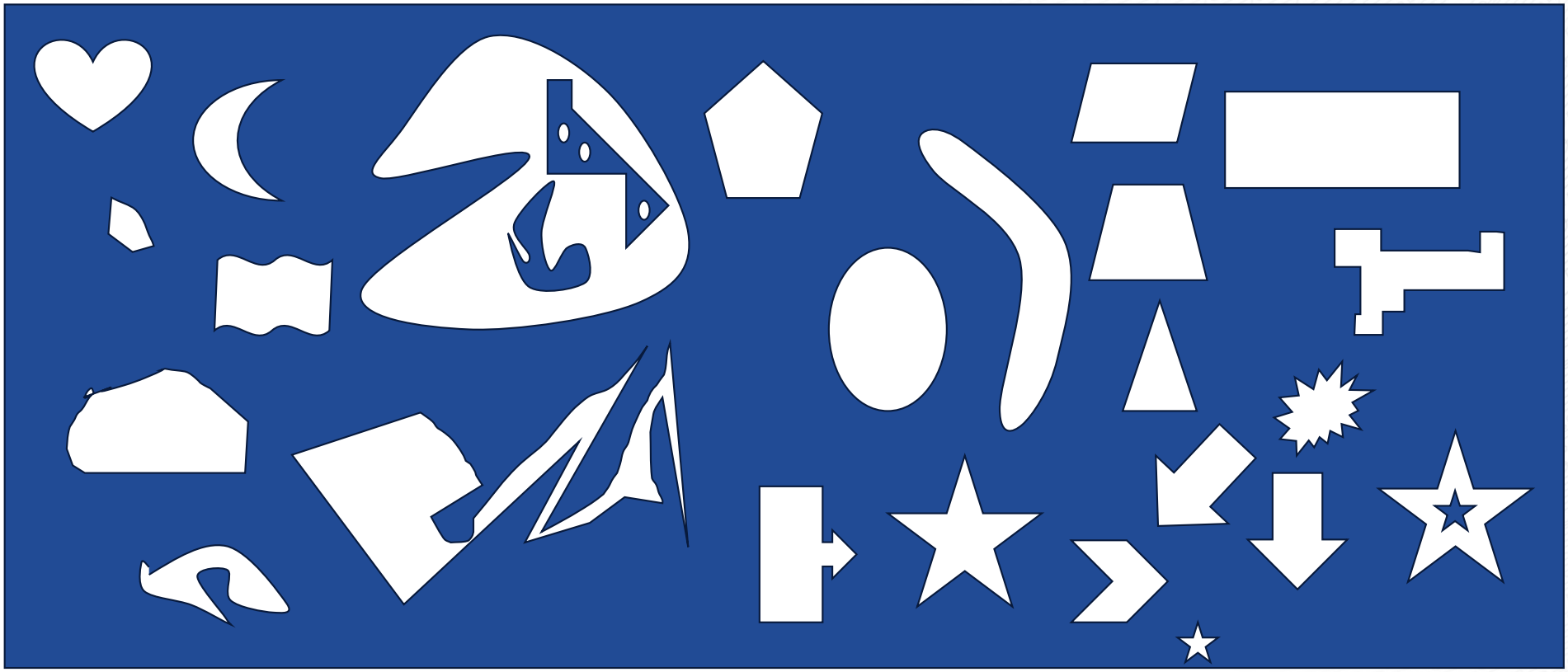
7



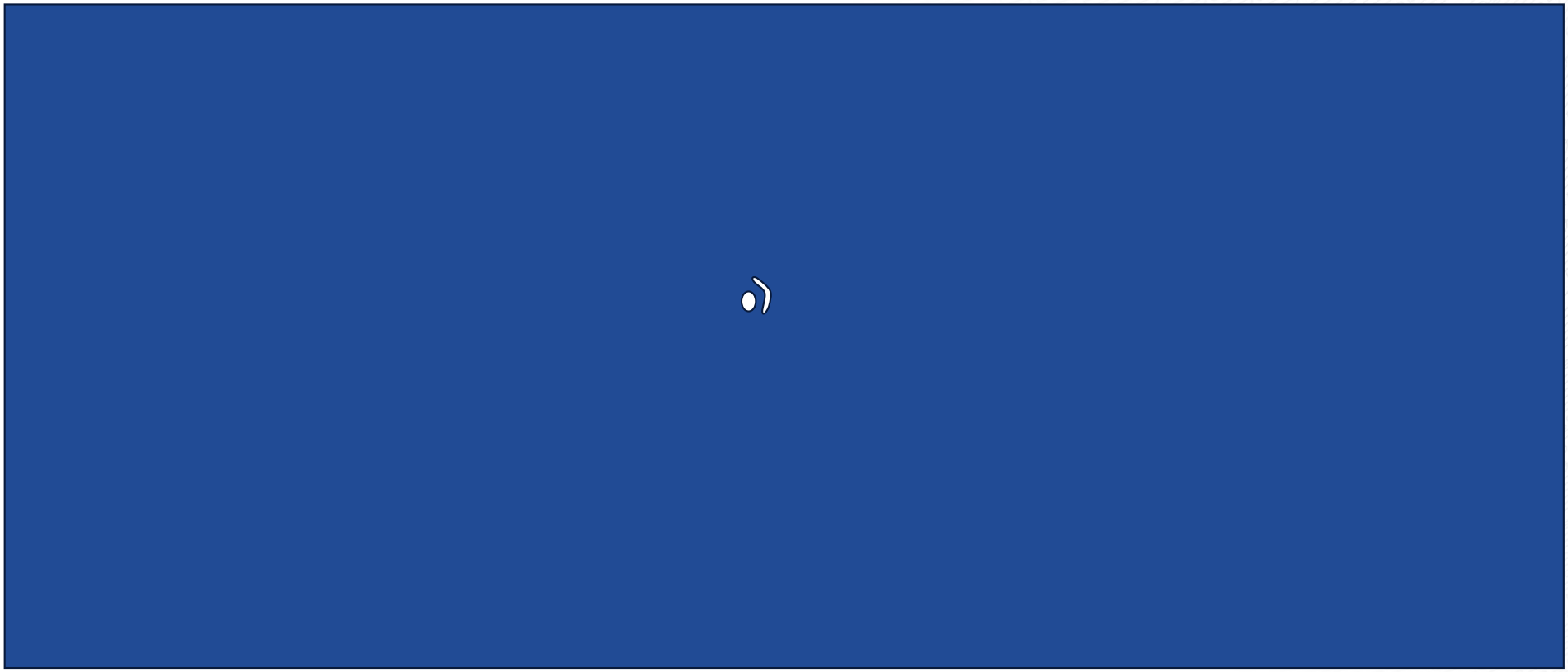
micron

"Curvilinear Masks in Memory for DUV and EUV", Ezequiel Russell, Micron, eBeam Initiative Reception, September 27, 2022

Space of all Shapes is Very Large

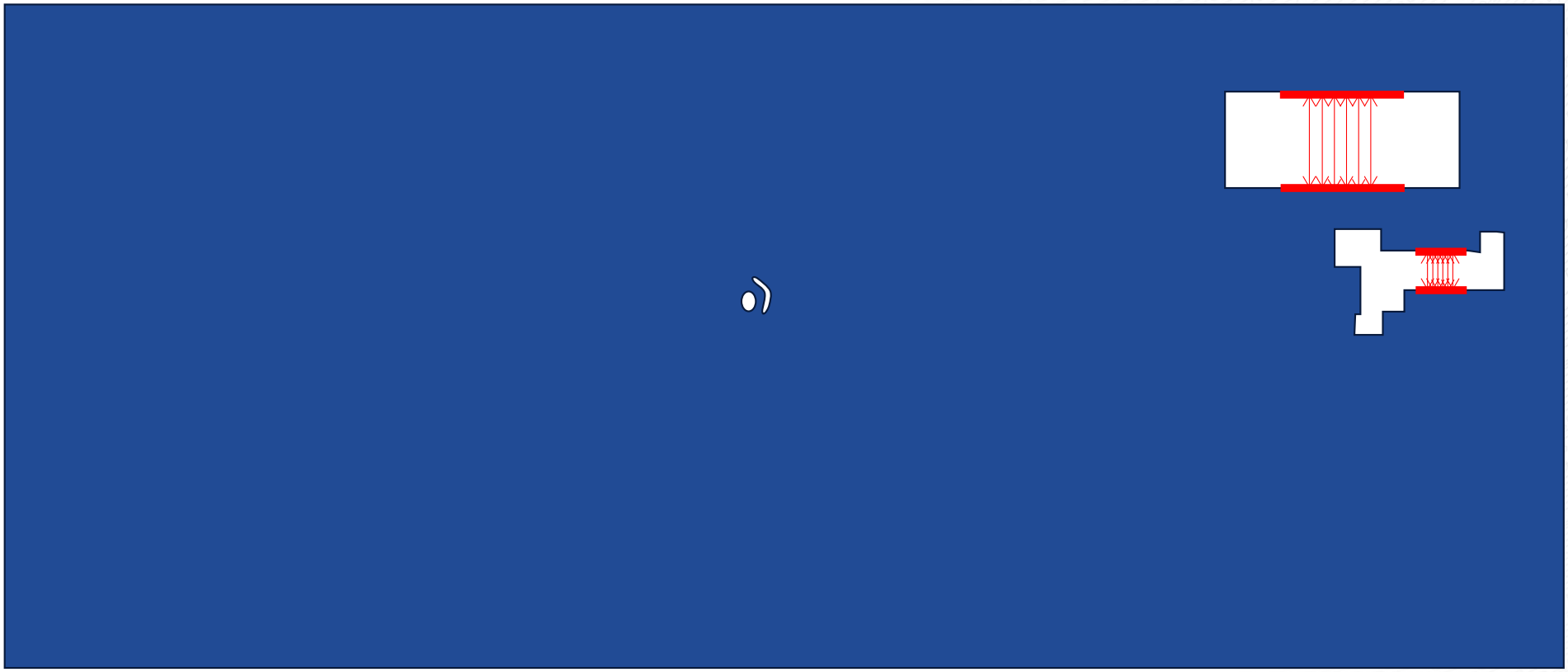


Space of All Manufacturable Curvilinear Shapes is Very Small



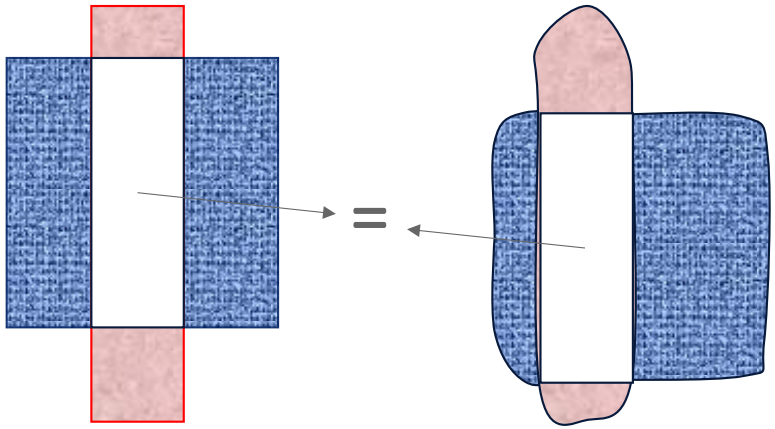
No Manhattan Shape is Manufacturable

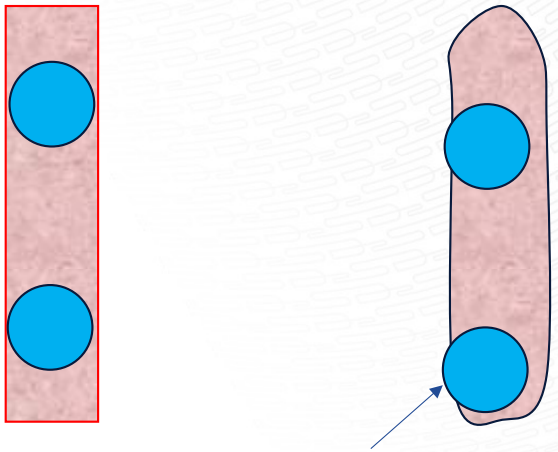
1D CD of Manhattan Shapes ARE Manufacturable



Wafer Designs are Made So Only 1D CD is Important

Design is resilient to misalignment and corner rounding





This is bad, but it's a compromise

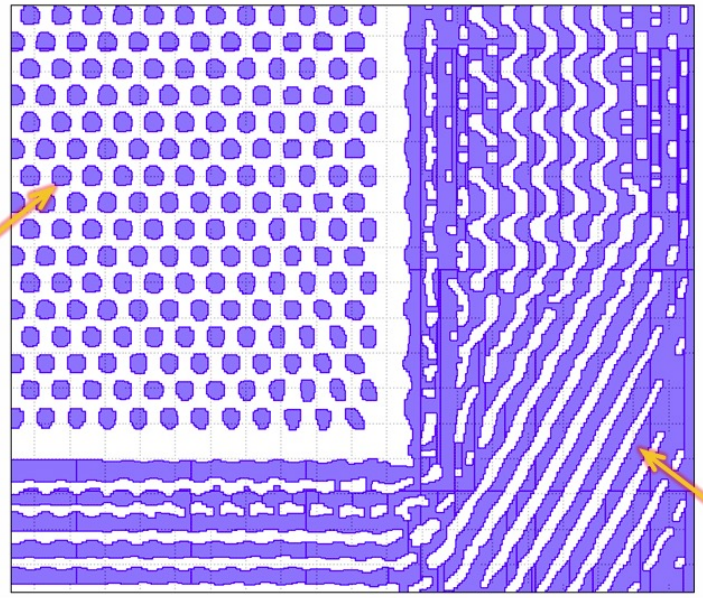
2D Matters on Mask, a lot

"Easiest way to improve CDU on wafer is to improve it on mask"

10

DRAM Array Core: Curvilinear ILT Correction

Improved NILS, CD Uniformity, and Contact Shape



Full-Chip ILT

- Application to a common DRAM array contact-like layer
  - CD uniformity and contact shape is critical

Mask Complexity

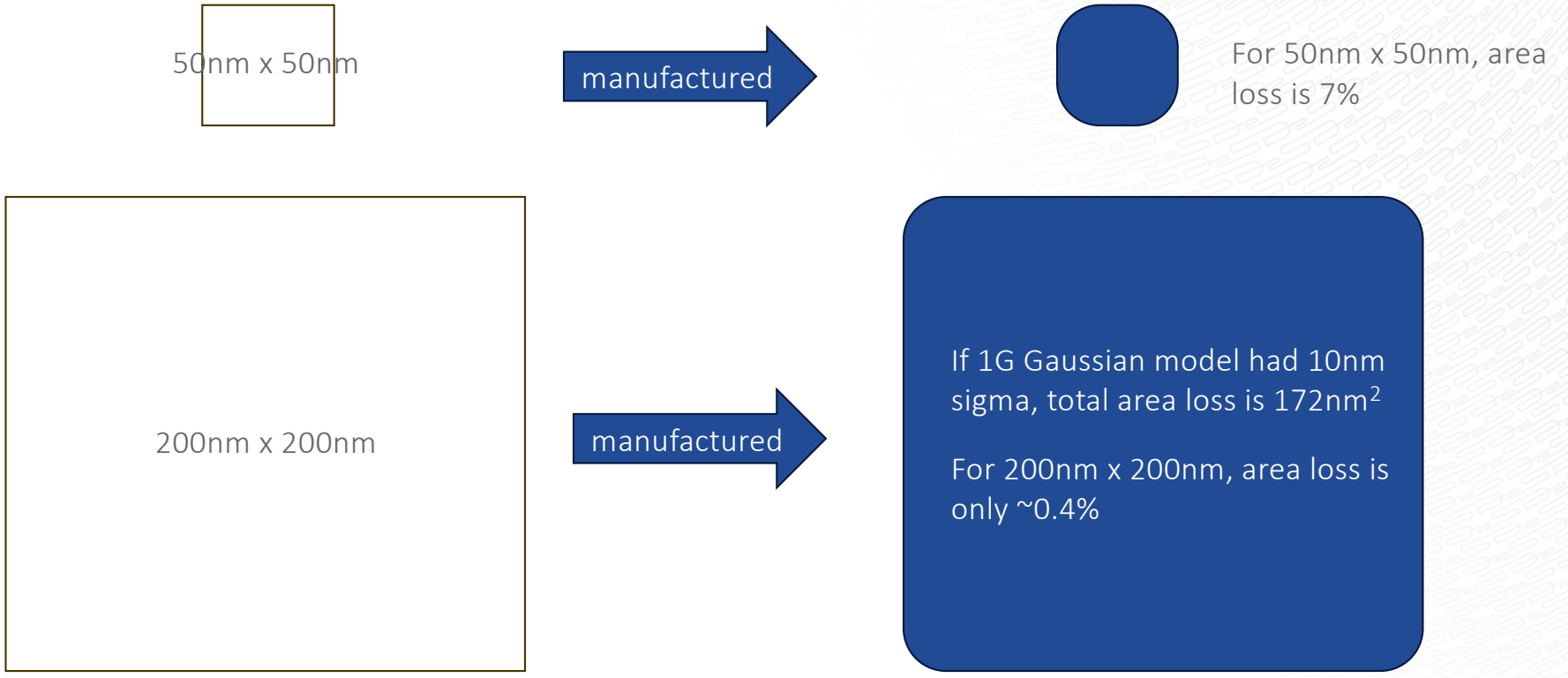
- Both Main features and assist features are curvilinear (small step Manhattanized) ILT

micron

Wafer Accuracy is About Area Accuracy on Mask

So smaller shapes we need to handle now can't be doing 1D

This is already true for all decorated OPC masks before Curvy…

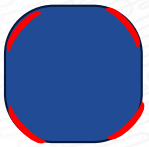


Dose Margin is Important

Instance-to-instance variation is critical for manufacturing

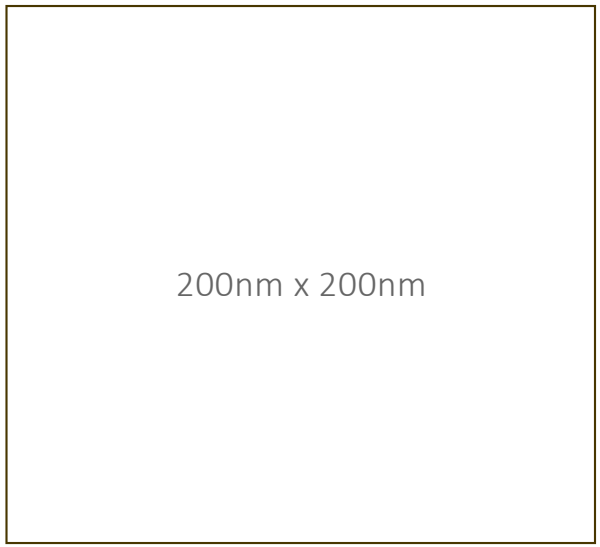
manufactured

Poor dose margin on corners

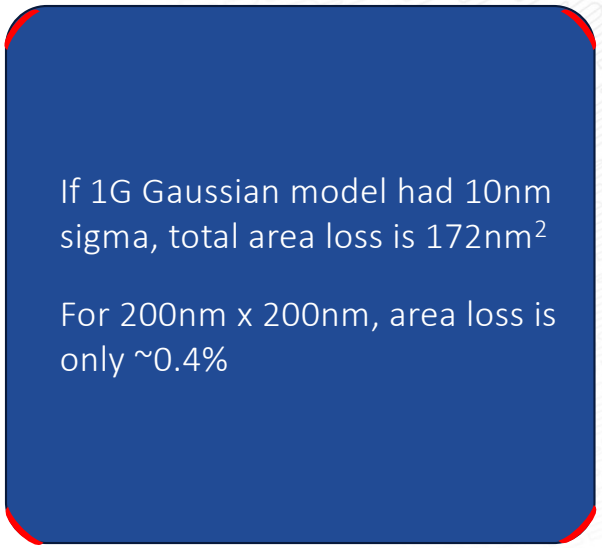


For 50nm x 50nm, area loss is ~~7~~%

6-8% depending on instance



manufactured

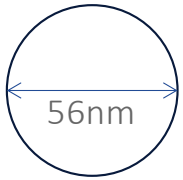


If 1G Gaussian model had 10nm sigma, total area loss is 172nm^2

For 200nm x 200nm, area loss is only ~0.4%

Much Better to Ask for What You can Get

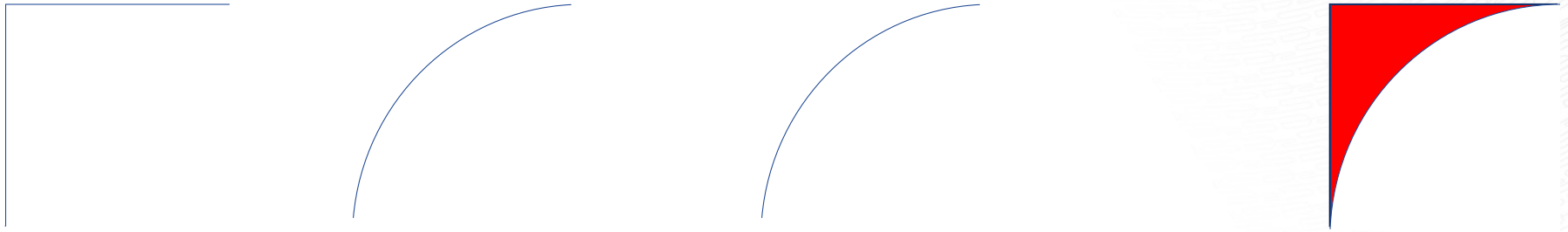
Instance-to-instance variation is critical for manufacturing



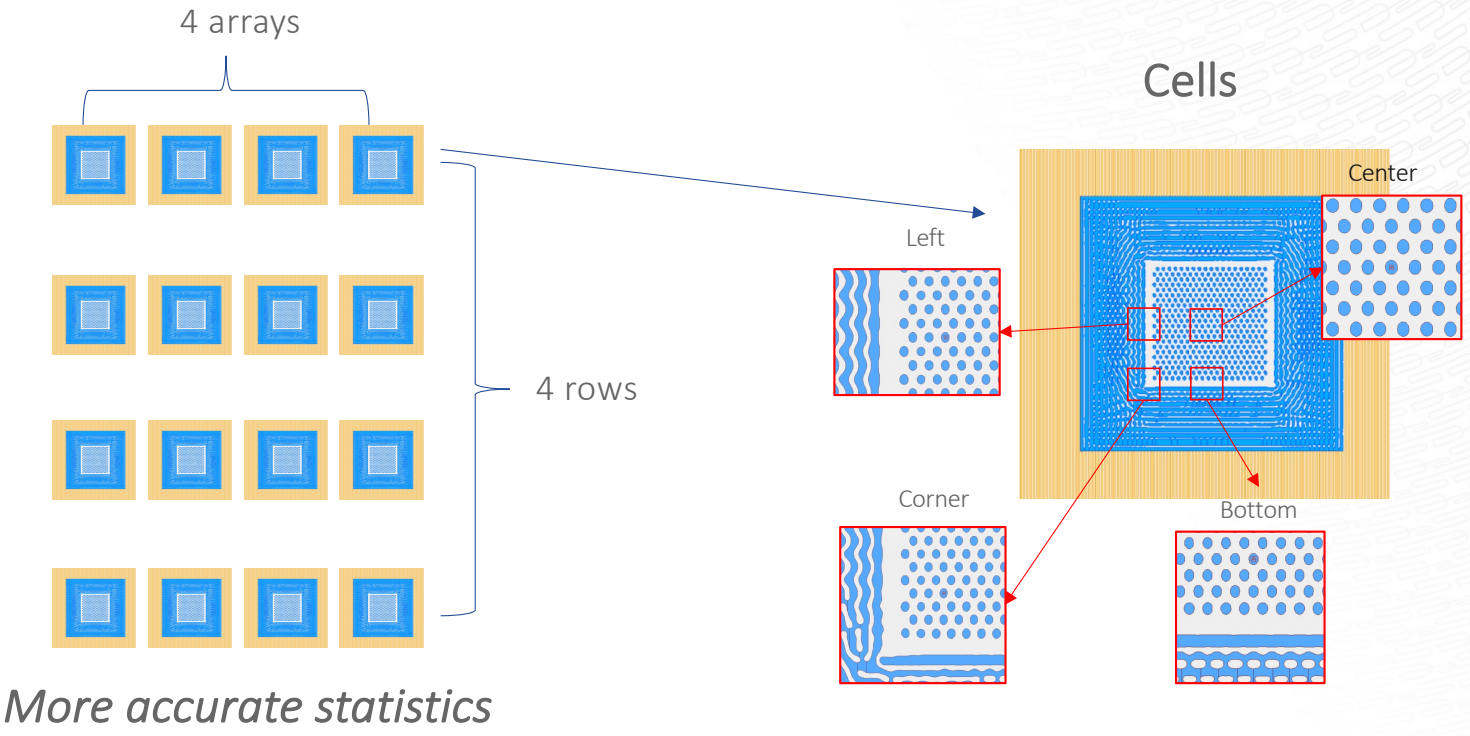
Better and uniform dose margin

No area loss in nominal
And less variation

Trying to manufacture this and getting this has more variation than trying to manufacture this because the dose of this area changing +/-x% makes a big difference.



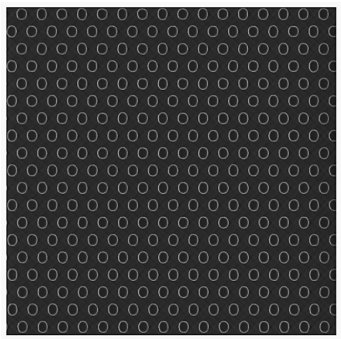
Study of Mask Variation with 16 Copies of Curvilinear Mask and Manhattan Mask Written by Multi Beam



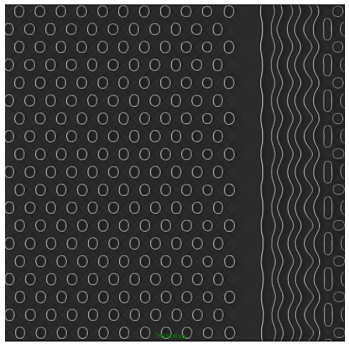
More accurate statistics

L. Pang, et. al, "Curvilinear Mask Metrology: What is the Equivalent CD? ", JM3 Curvilinear Mask Special Edition

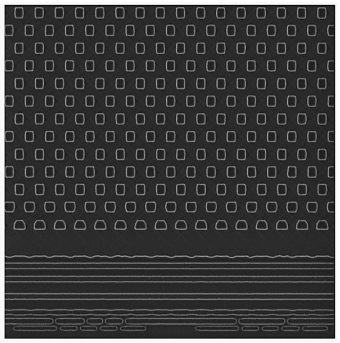
SEM Images are Collected for 4 Locations of Contact Array



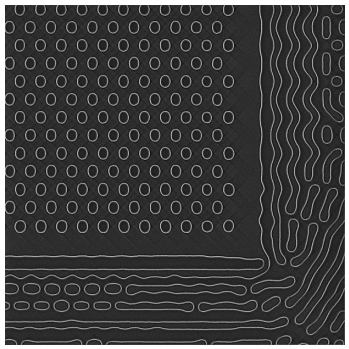
Center



Left (mirrored)

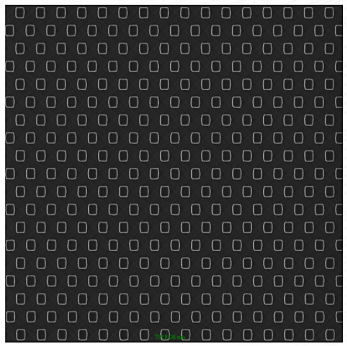


Bottom

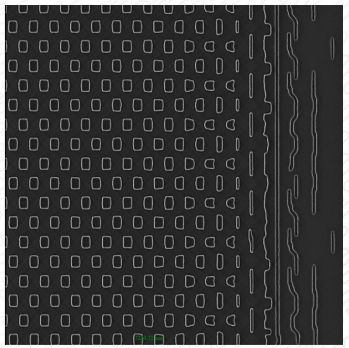


Corner

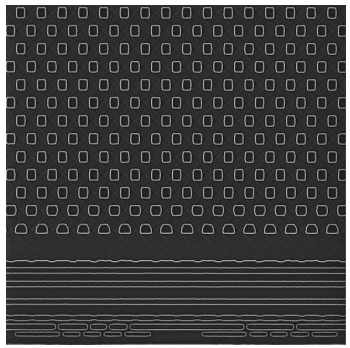
Curvilinear



Center



Left (mirrored)



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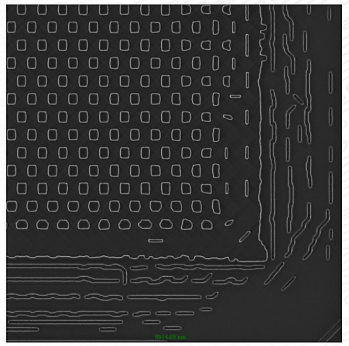
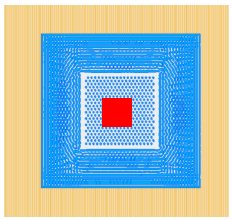


Corner

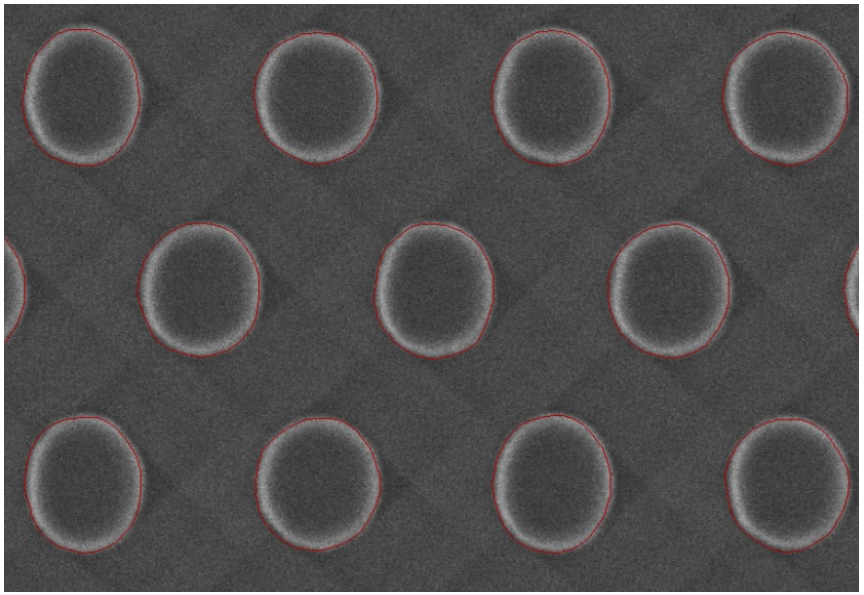
Manhattan

L. Pang, et. al, “Curvilinear Mask Metrology: What is the Equivalent CD? “, JM3 Curvilinear Mask Special Edition
SEM Courtesv : Micron

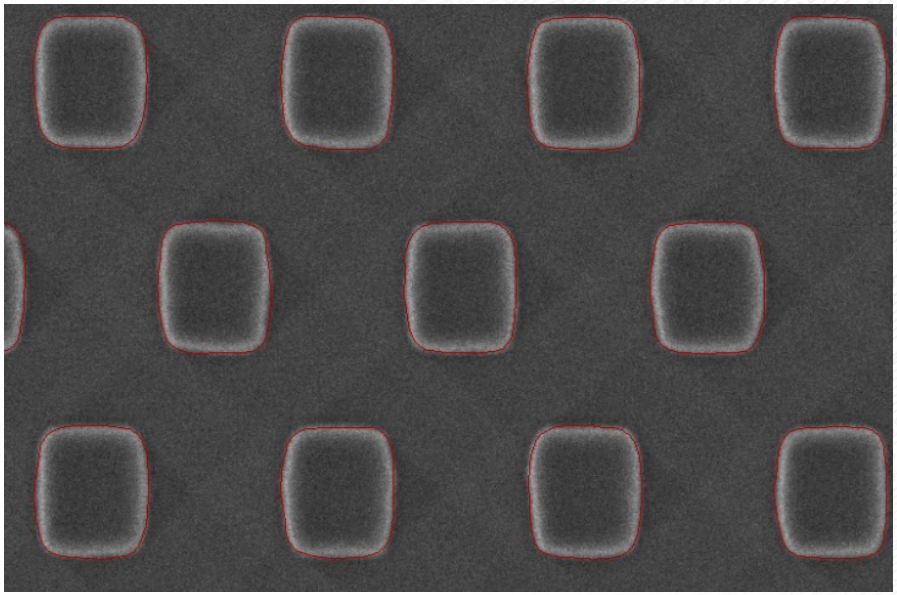
For Each Location 16 SEM Images are Aligned and Contours are Extracted to Form Variation Band



Center: Mask Contours Extracted



Curvilinear Mask Pattern

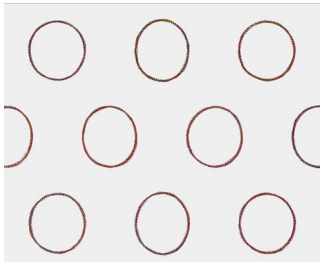


Manhattan Mask Pattern

L. Pang, et. al, “Curvilinear Mask Metrology: What is the Equivalent CD? “, JM3 Curvilinear Mask Special Edition
SEM Courtesv : Micron

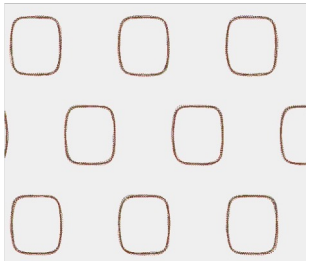
Curvilinear Reduced Mask Variation by ~20%

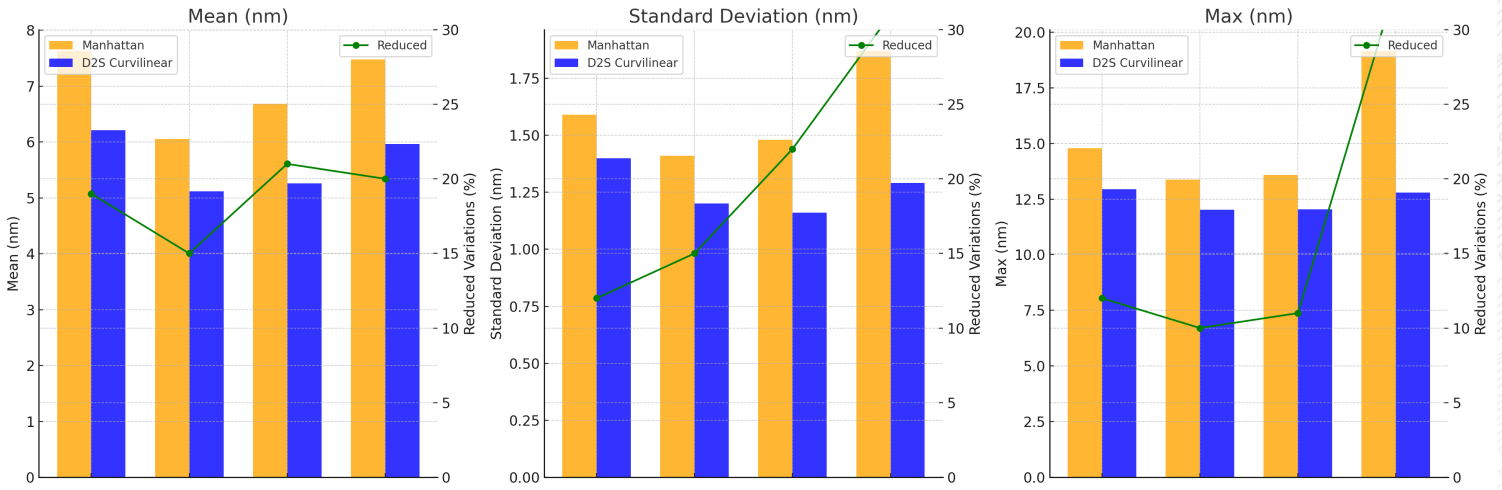
This will translate to wafer variation on every chip



Aligned D2S Curvilinear Mask Contours

Blue: Curvilinear
Orange: Manhattan

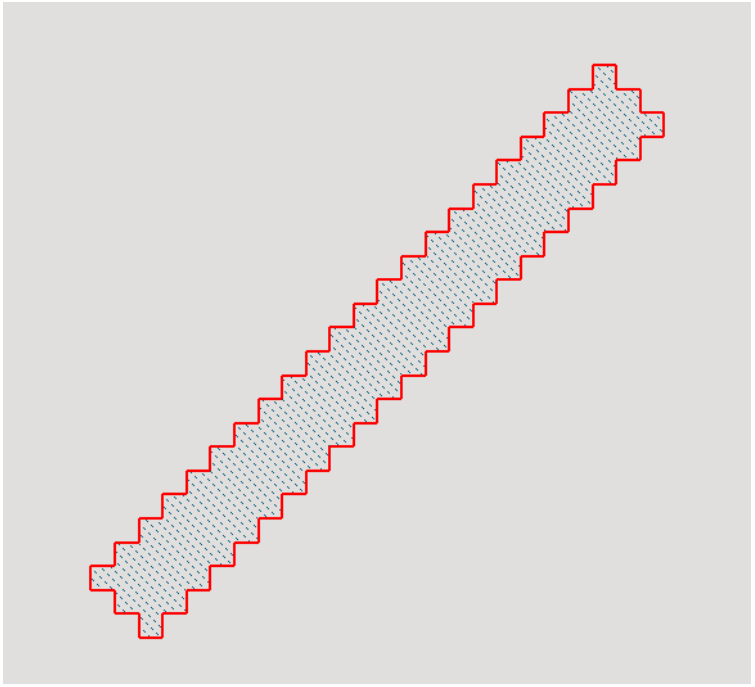




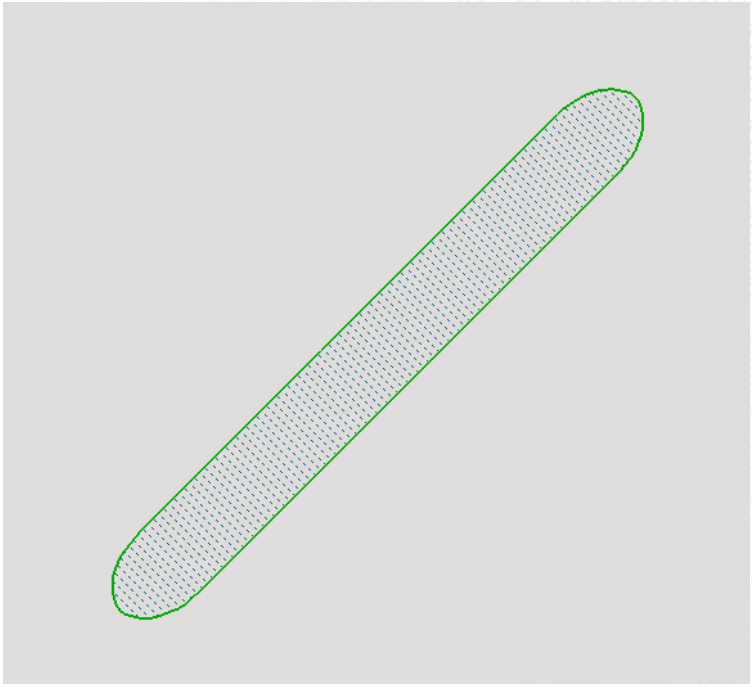
L. Pang, et. al, “Curvilinear Mask Metrology: What is the Equivalent CD? “, JM3 Curvilinear Mask Special Edition

Let’s Look at MEEF : Mask Effect on Wafer

MEEF: Mask Error Enhancement Factor

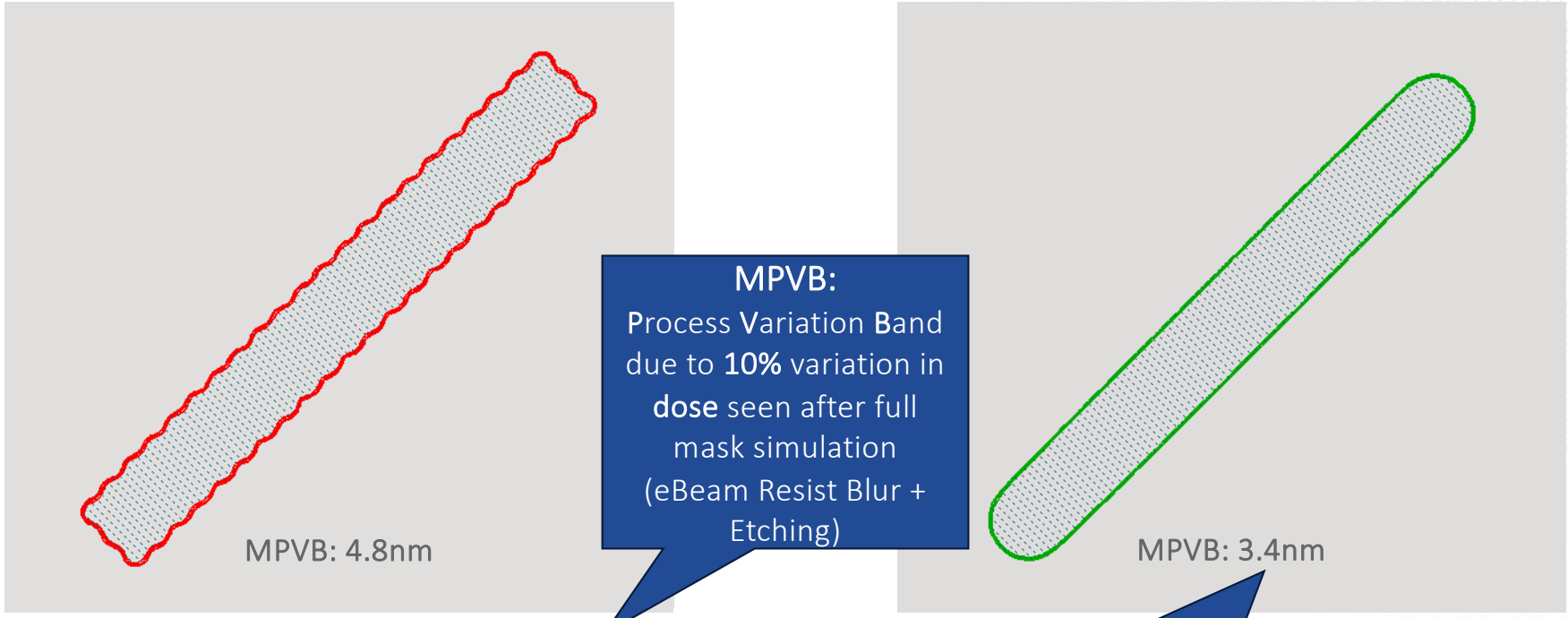


Design Width
144 nm (Mask)
36 nm (Wafer)



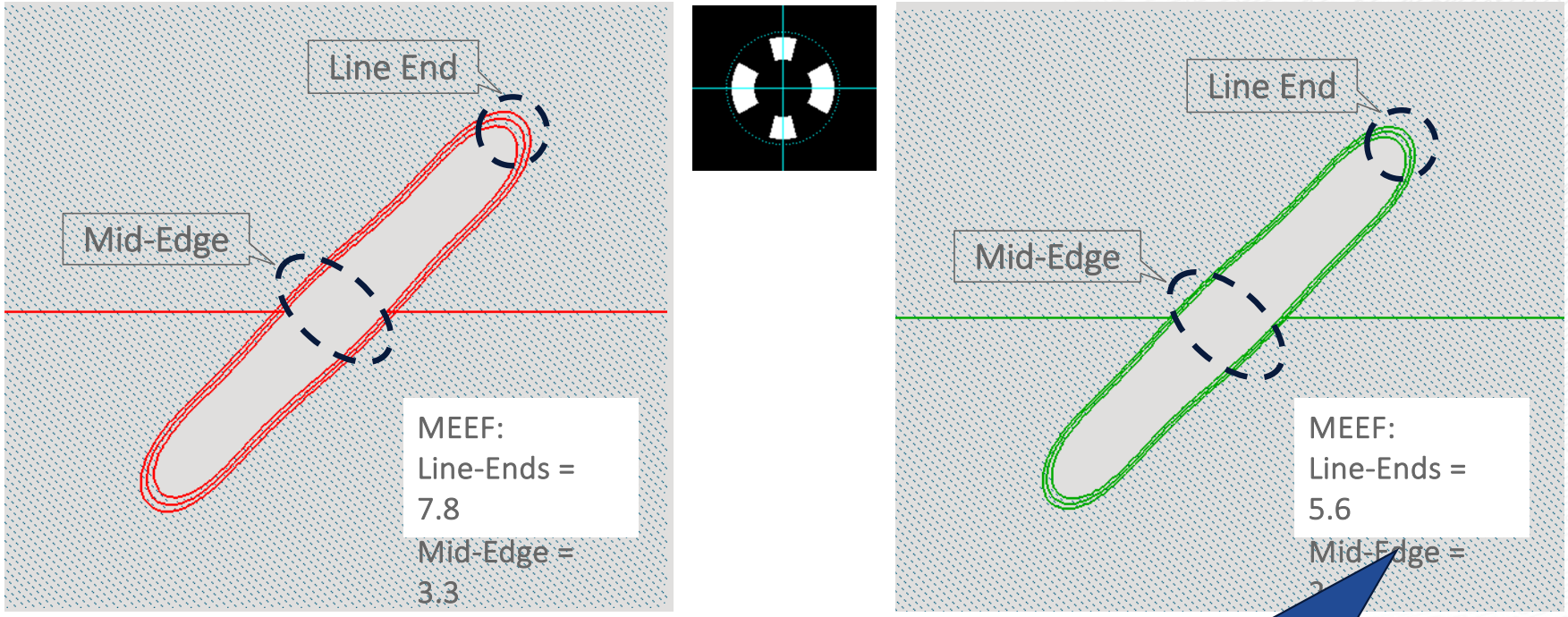
Abhishek Shendre, et al, “Leaping into the Curvy World with GPU-Accelerated O(p) Computing,”, BACUS 2024, SPIE 12751-10

Smooth Diagonals Are More Manufacturable On Mask



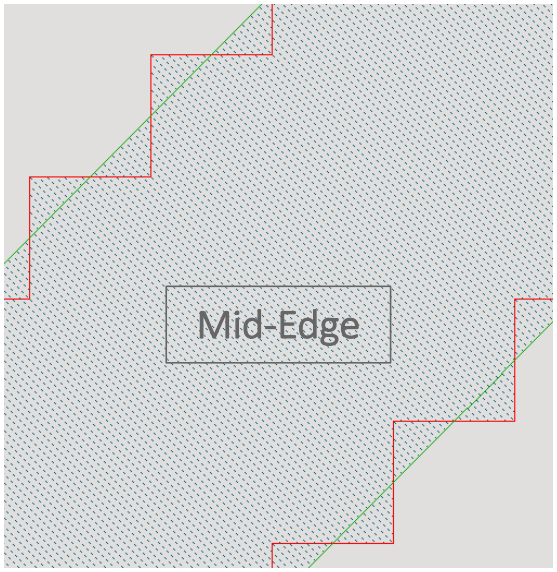
And Smooth Diagonals Provide Better MEEF

193i with 1.35 NA and a composite light source sigma: 0.5 (inner) 0.9 (outer) and TE polarization

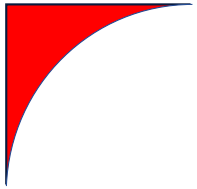


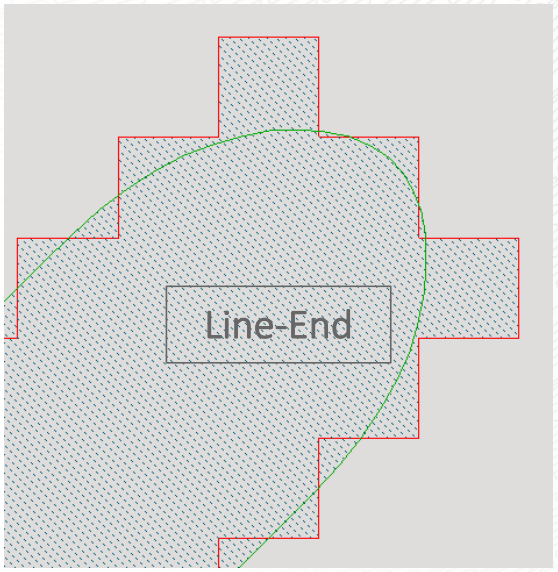
MEEF: Mask Error Enhancement Factor

Manufacturable Shapes are More Reliably Manufactured



Remember this?





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Ask for What You Can Get

And Get What You Asked For

This should guide what we mean by “curvilinear”

Curvy Masks and GP-GPUs Both Started in 2006

Got Enabled by Multi-Beam Mask Writing

2006 — ILT Introduced

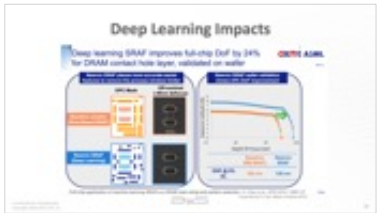
2009 — Overlapping Shots enabled by GPU acceleration

2015/16 — Multi-beam Mask Writers

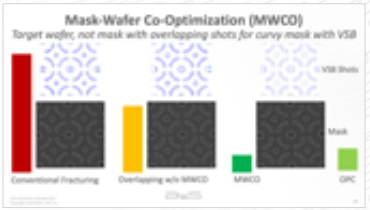
2017 — Curvy Good For EUV, too

2019 — Full-Chip Curvy ILT enabled by GPU acceleration

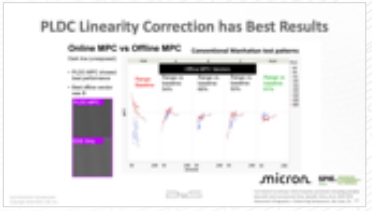
Deep Learning enabled by GPUs



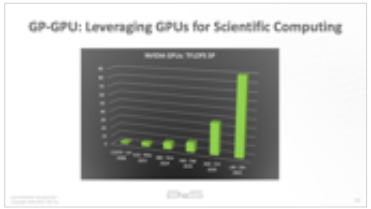
2020 — MWCO enabled by GPU acceleration



2025 — Curvy Mask Solution enabled by GPU acceleration (PLDC)



GP-GPU Computing



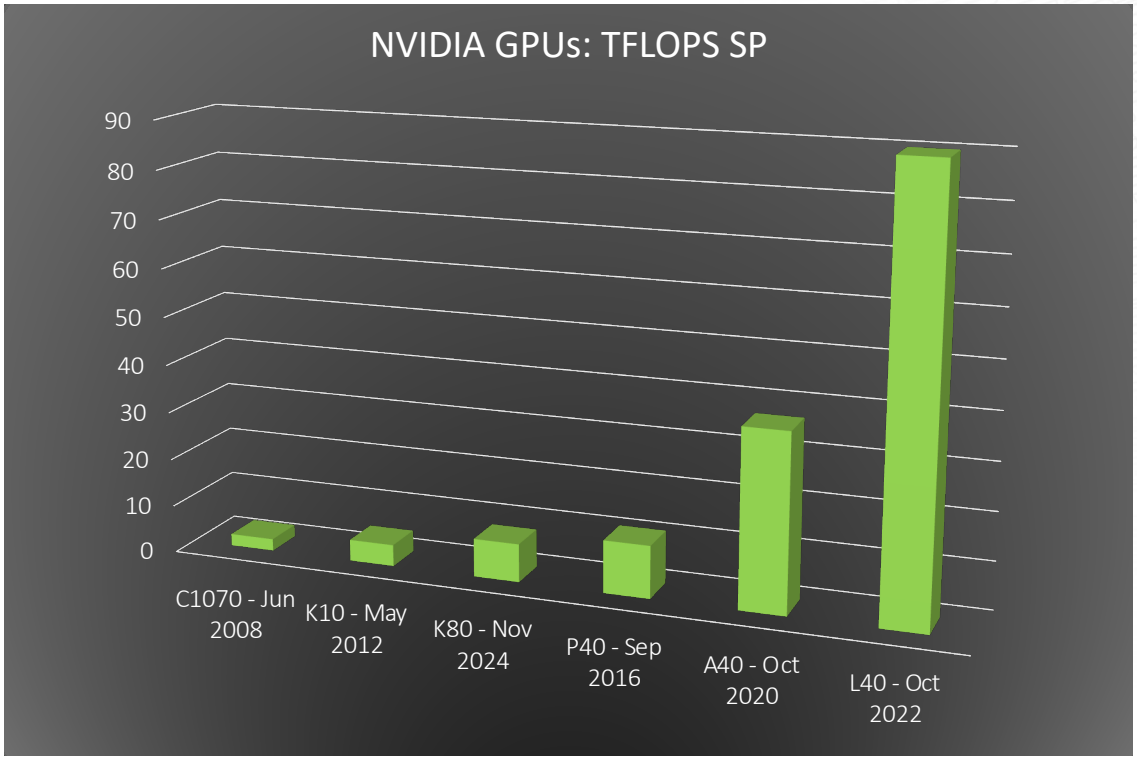
Luminesent Introduced ILT

Fast Inverse Lithography Technology

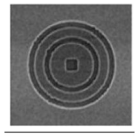
Daniel S. Abrams, Linyong Pang
Luminescent Technologies, Inc., 650 Castro Street, Suite 220, Mountain View, CA 94041, U.S.A.

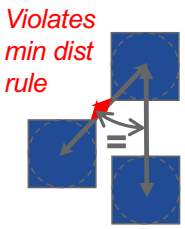
1. Abrams, Daniel S., and Linyong Pang. "Fast inverse lithography technology." In *Optical Microlithography XIX*, vol. 6154, p. 61541J. International Society for Optics and Photonics, 2006.

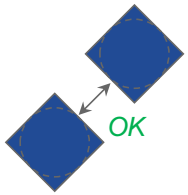
GP-GPU: Leveraging GPUs for Scientific Computing

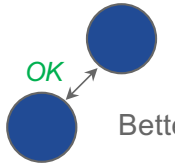


Overlapping Circles = Smooth Curvilinear Features with Fewer Shots



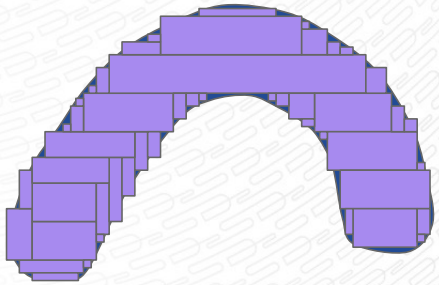




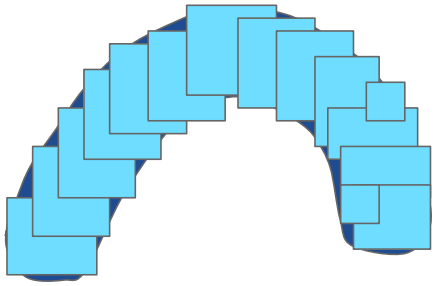


Better MEEF

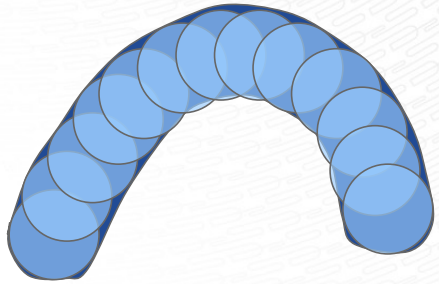
Target Shape



40 Conventional VSB Shots



15 Overlapping VSB Shots

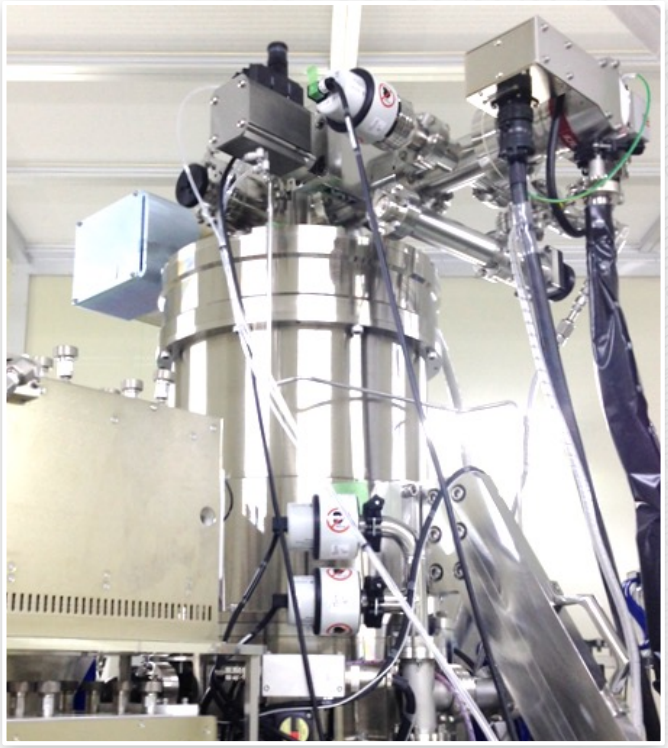


13 Overlapping Circles

Multi-Beam Mask Writers Introduced

Prototype pictured. eBeam Initiative presentation 2015

IMS Nanofabrication



Prototype pictured. eBeam Initiative presentation 2016

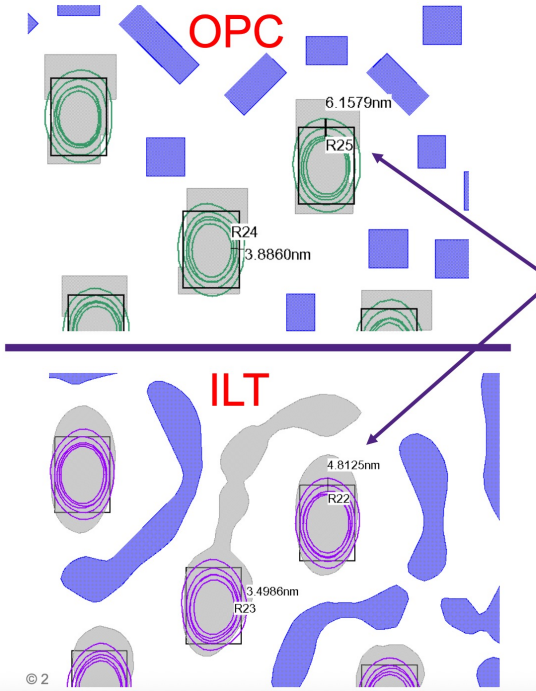
NuFLARE

D2S

Curvy Is Good for EUV, Too

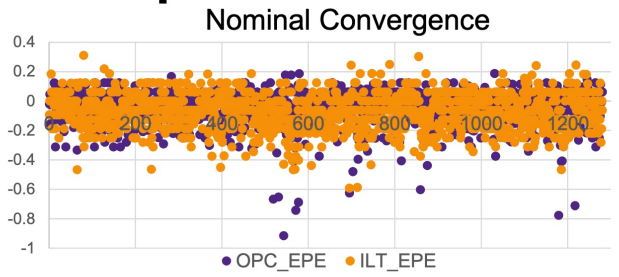
EUV Via Random Pattern – PV Band Improvement

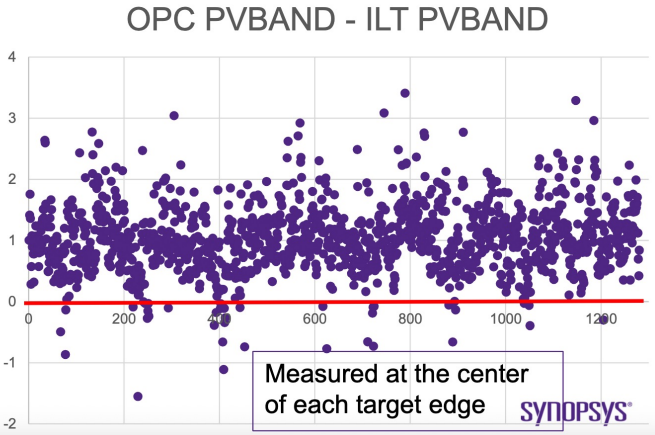
ILT Improves PV Band by > 20%



PV band measuring spread of
- +/-15% dose
- +/- 50 nm focus

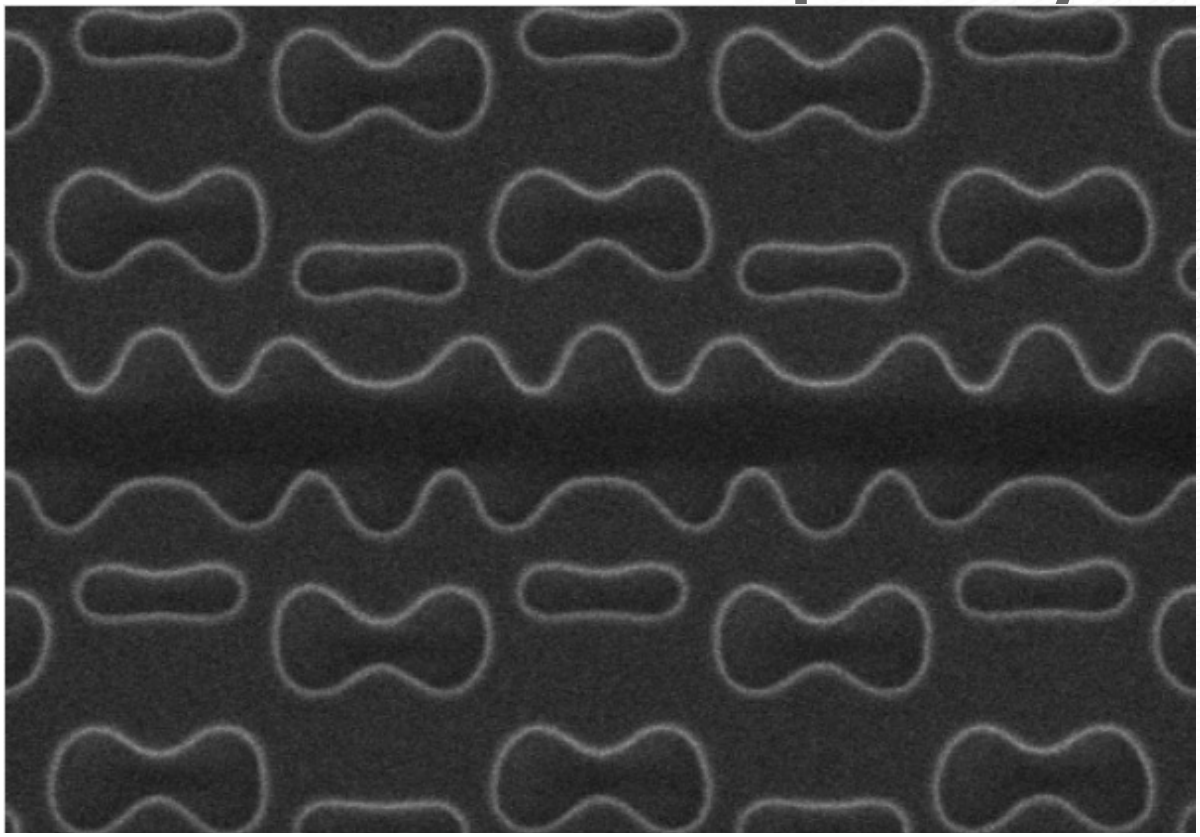
ILT Improvement





Presented by Tom Cecil at eBeam Initiative 2017

TrueMask® ILT: Full-Chip Curvy ILT



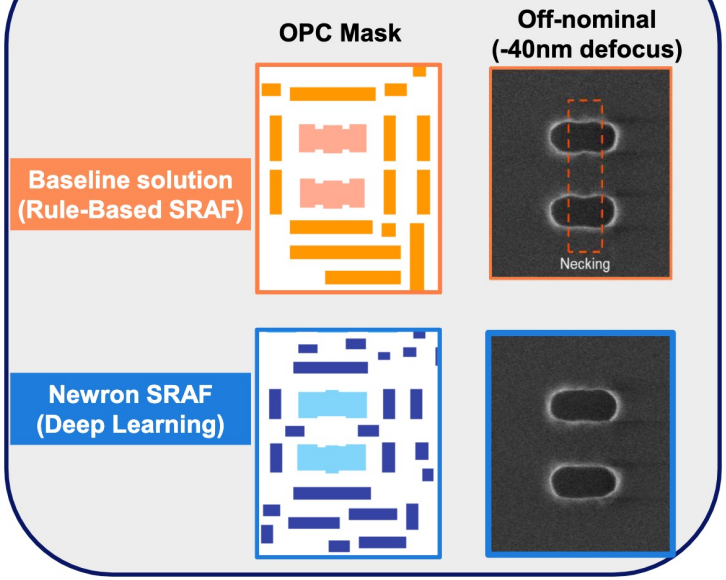
Deep Learning Impacts

Deep learning SRAF improves full-chip DoF by 24% for DRAM contact hole layer, validated on wafer

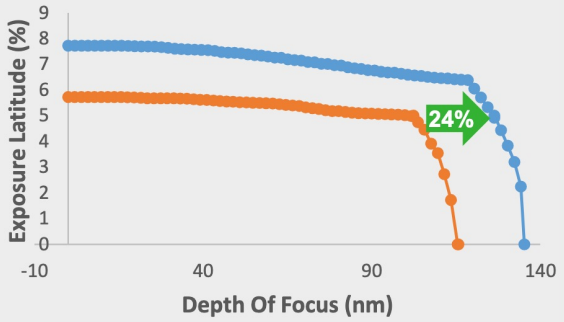
cxmt ASML

Slide 13

Newron SRAF places more accurate assist features to remove the process window limiter



Newron SRAF wafer validation shows 24% DoF improvement



	Baseline (RB-SRAF)	Newron SRAF
DOF @ 5% EL	102 nm	126 nm

Full-chip application of machine learning SRAFs on DRAM case using auto pattern selection K. Chen et al., SPIE 2019, 10961-37

Public

Presented by Yu Cao, eBeam Initiative 2019

Mask-Wafer Co-Optimization (MWCO)

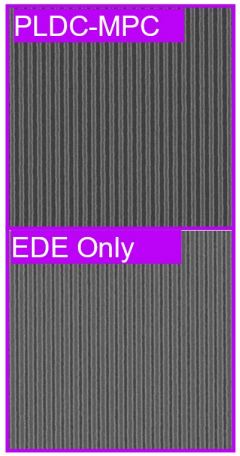
Target wafer, not mask with overlapping shots for curvy mask with VSB

PLDC Linearity Correction has Best Results

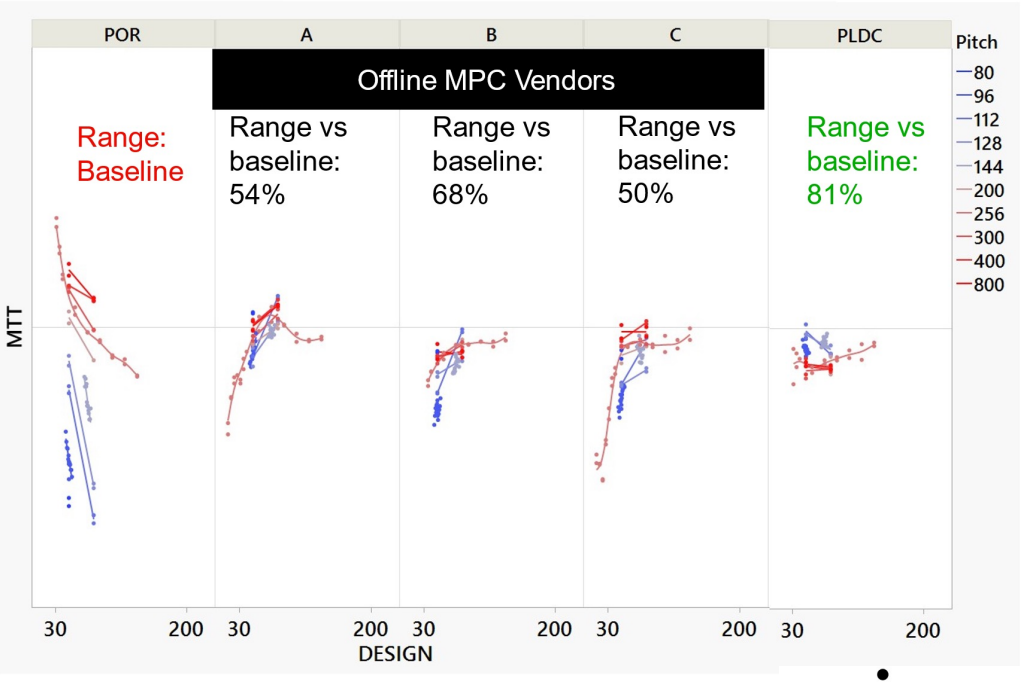
Online MPC vs Offline MPC

Dark line (unexposed)

- PLDC-MPC showed best performance
- Best offline vendor was B



Conventional Manhattan test patterns



micron SPIE. ADVANCED LITHOGRAPHY+ PATTERNING 2025

Full-reticle Curvilinear inline linearity correction including variable bias with zero turnaround time, Spinelli, Paris, et al, 2025 SPIE Advanced Lithography + Patterning Symposium, San Jose, CA

So Curvilinear Masks Can be Manufactured

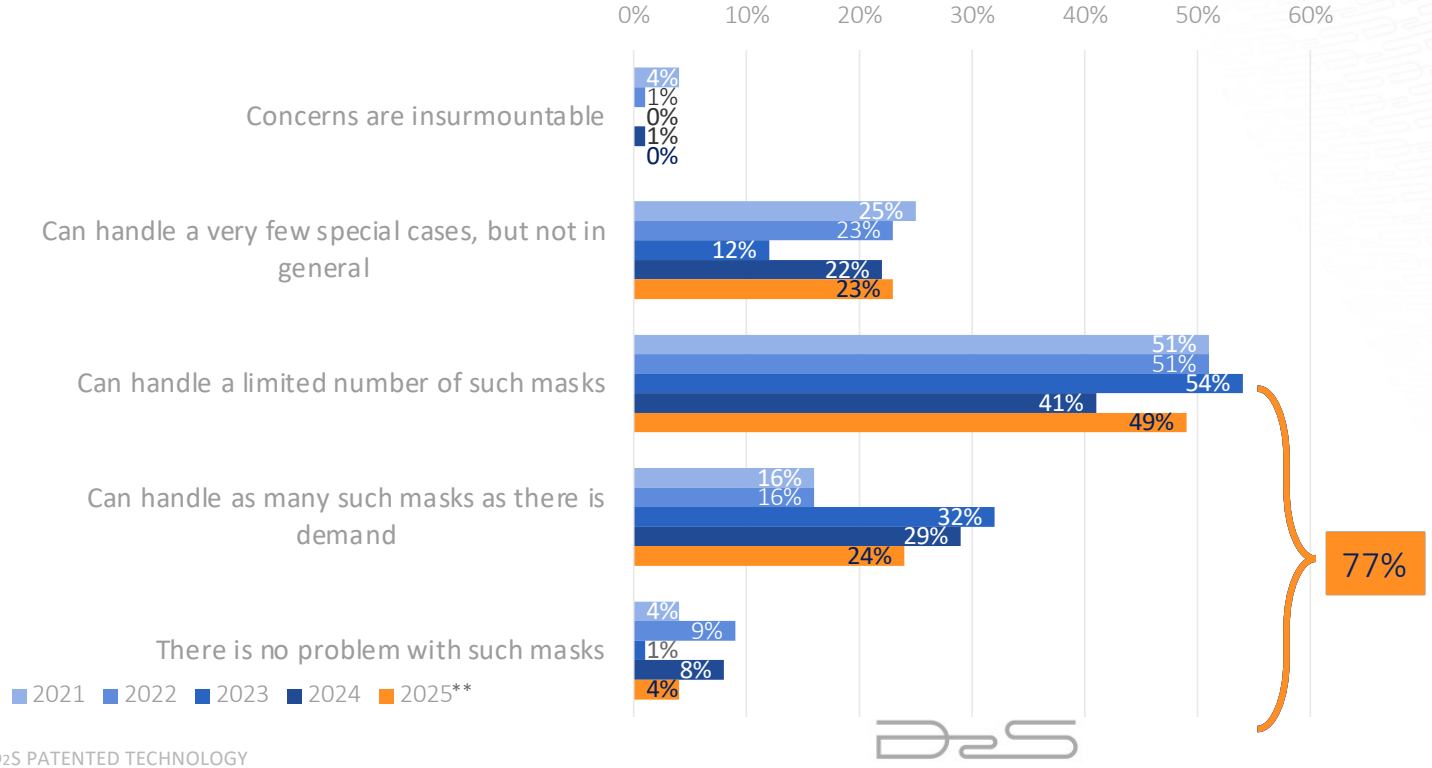
And it's better for wafer process window

Any other barriers to adoption?

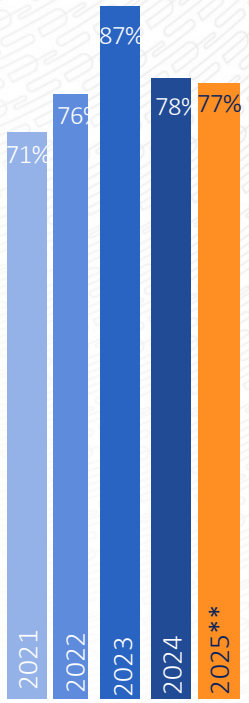
Confidence Remains High for Curvilinear

But reality may be setting in on some barriers

eBeam Initiative Luminaries Surveys 2021-2025:**
Are the problems with HVM of masks containing curvilinear features insurmountable for leading-edge mask shops by the end of next year? Select the statement that you agree with most.



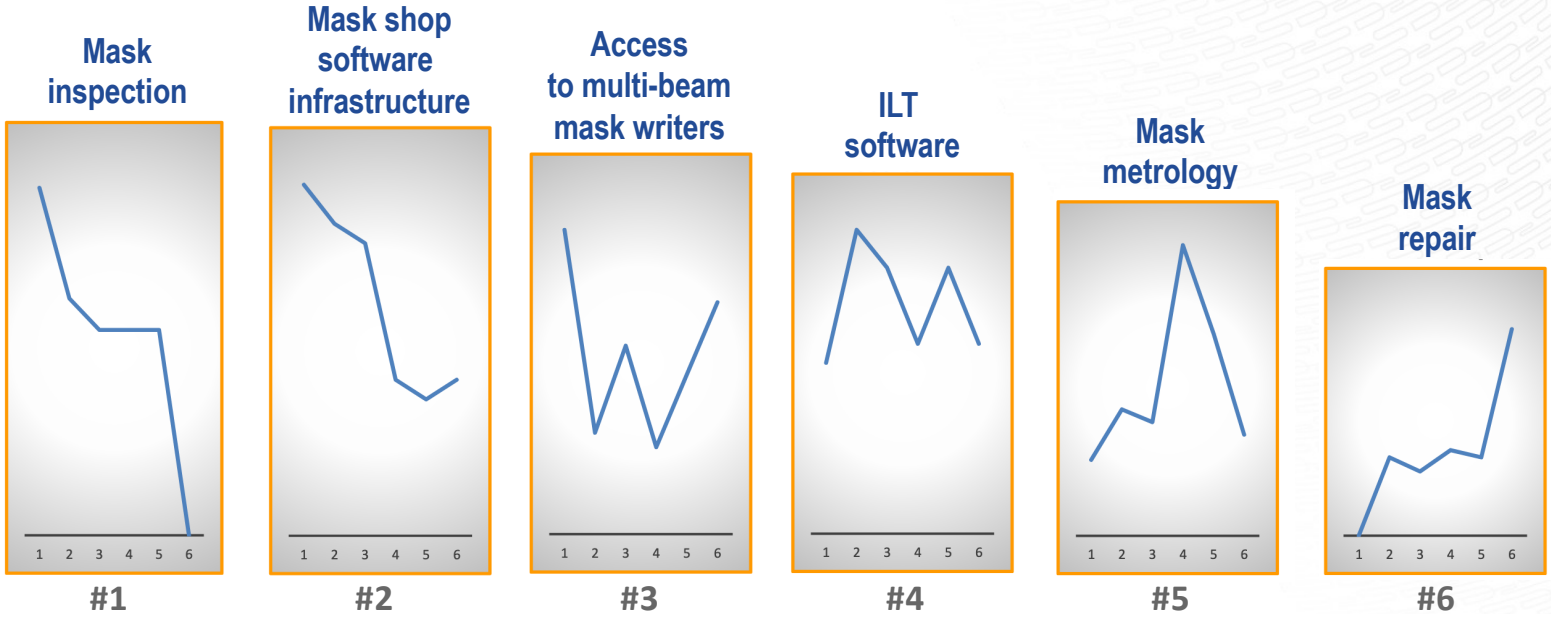
At least a limited number of masks being curvy is okay for leading-edge mask shops:



**Preliminary results. Full 2025 survey results available eBeam Initiative Event on Sept. 23 or ebeam.org

Views of Challenges Change: 2021-2025**

eBeam Initiative Luminaries Surveys 2021-2025:
Please rank your biggest concerns in producing curvilinear masks

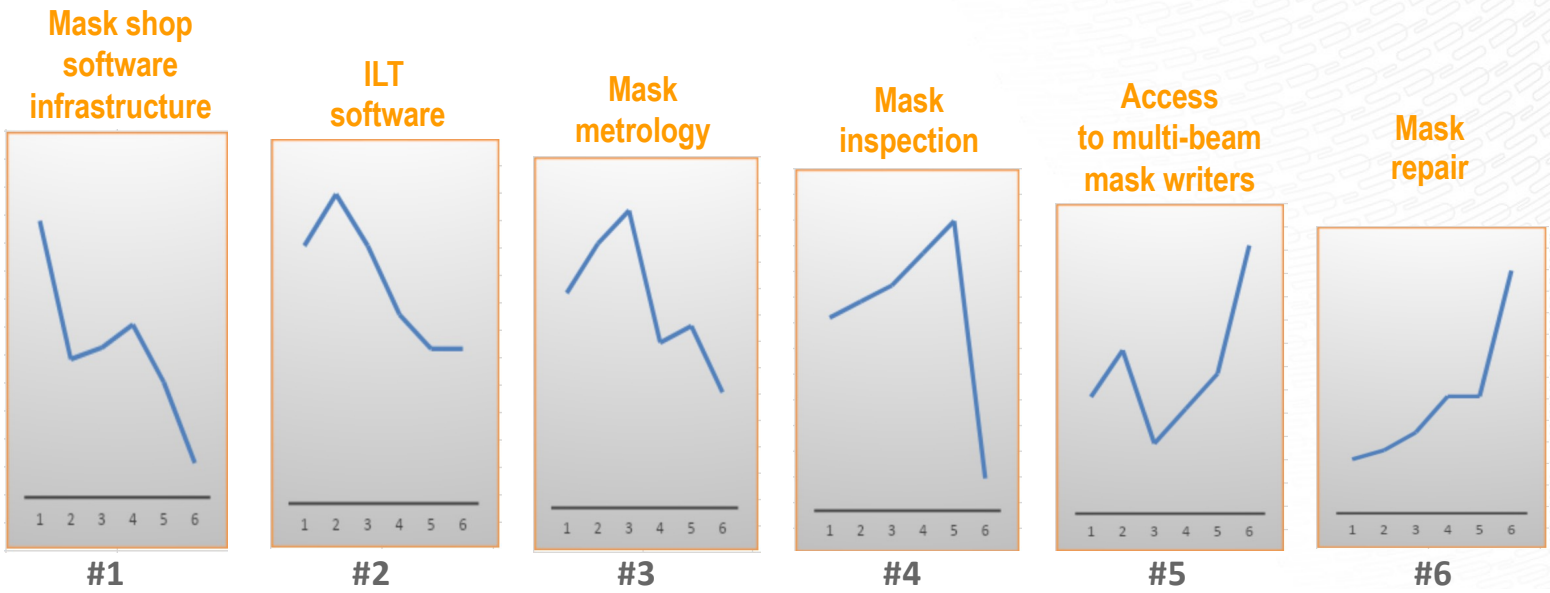


Note: 1-6 on X-axis indicate # of respondents that ranked that question as that ordinal number with 1 = highest

**Preliminary results. Full 2025 survey results available eBeam Initiative Event on Sept. 23 or ebeam.org

Views of Challenges Change: 2021-2025**

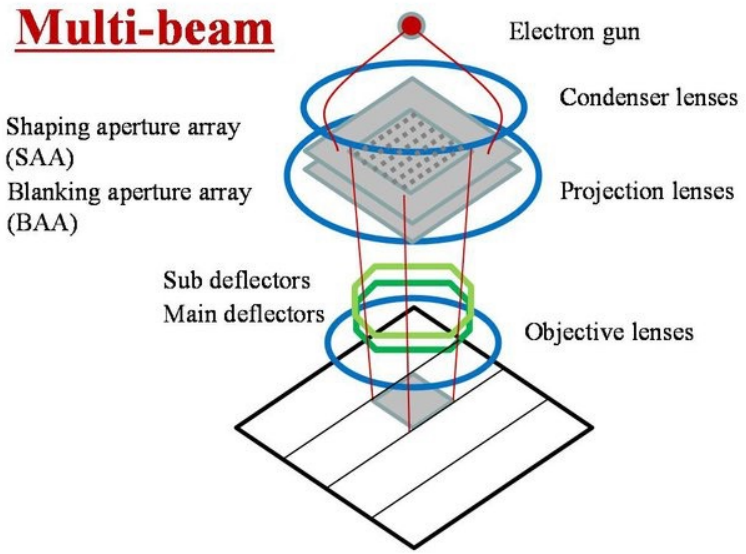
eBeam Initiative Luminaries Surveys 2025:
Please rank your biggest concerns in producing curvilinear masks



Note: 1-6 on X-axis indicate # of respondents that ranked that question as that ordinal number with 1 = highest

**Preliminary results. Full 2025 survey results available eBeam Initiative Event on Sept. 23 or ebeam.org

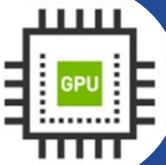
Pixel Based Computing With GPU Acceleration Is Natural For Multi-beam Writers



$O(p)$ Runtime Is Bounded By Number of Pixels

Algorithms Are Extremely SIMD

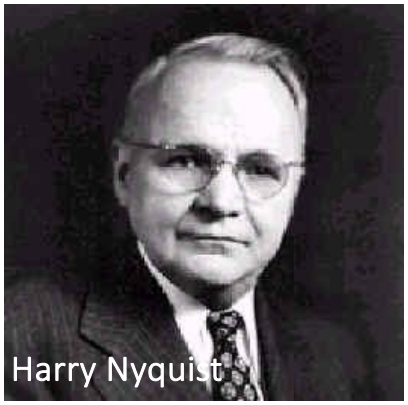
SIMD: Single-Instruction Multiple Data

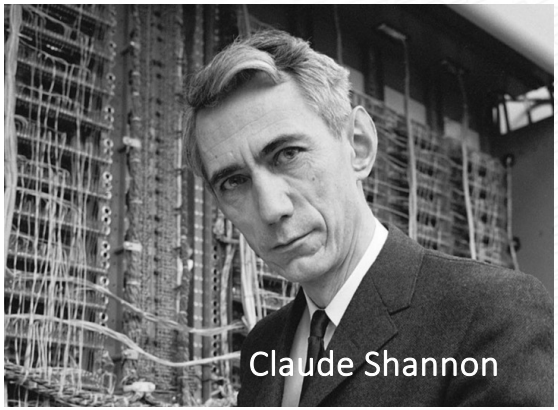


Highly Efficient With GPUs

Abhishek Shendre, et al, "Leaping into the Curvy World with GPU-Accelerated O(p) Computing,", BACUS 2024, SPIE 12751-10

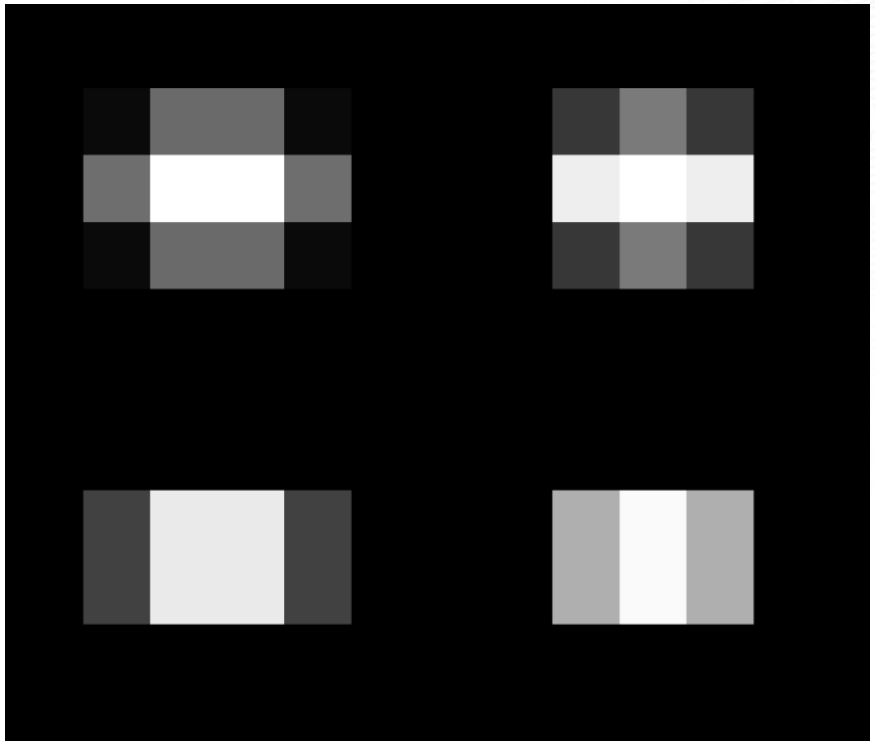
Rasterization is a Digital Sampling of Vector Shapes





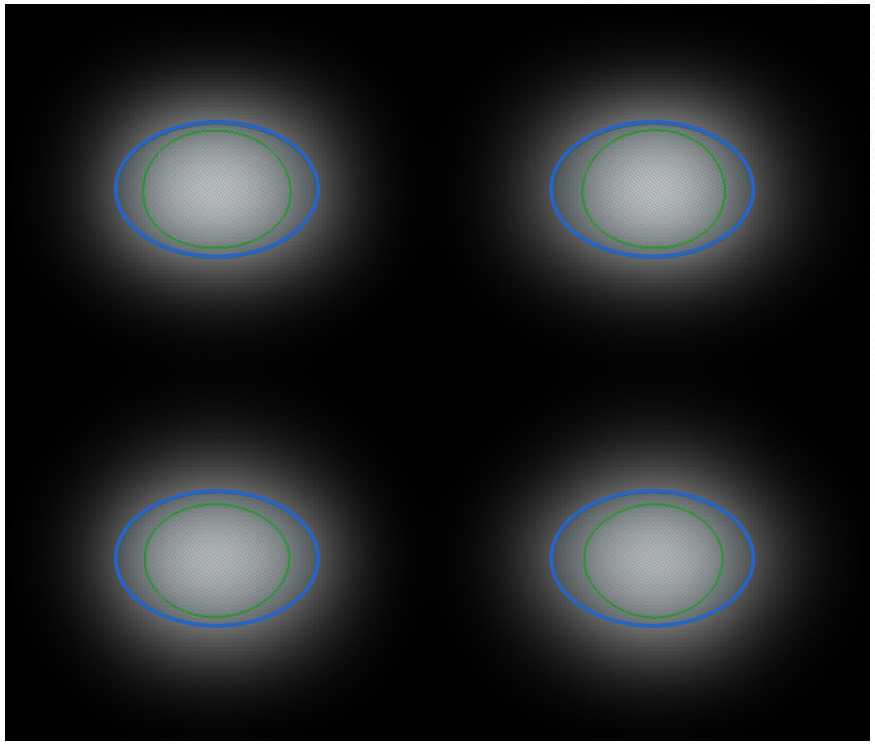
- Rasterization is 2D sampling of spatial information
  - Shannon-Nyquist sampling of 1D audio data from WW II in 2D
- Magic of rasterization creates smooth curves by low-pass filtering of the processes

Guess What Shapes These Pixels Represent?



Abhishek Shendre, et al, “Leaping into the Curvy World with GPU-Accelerated O(p) Computing,”, BACUS 2024, SPIE 12751-10

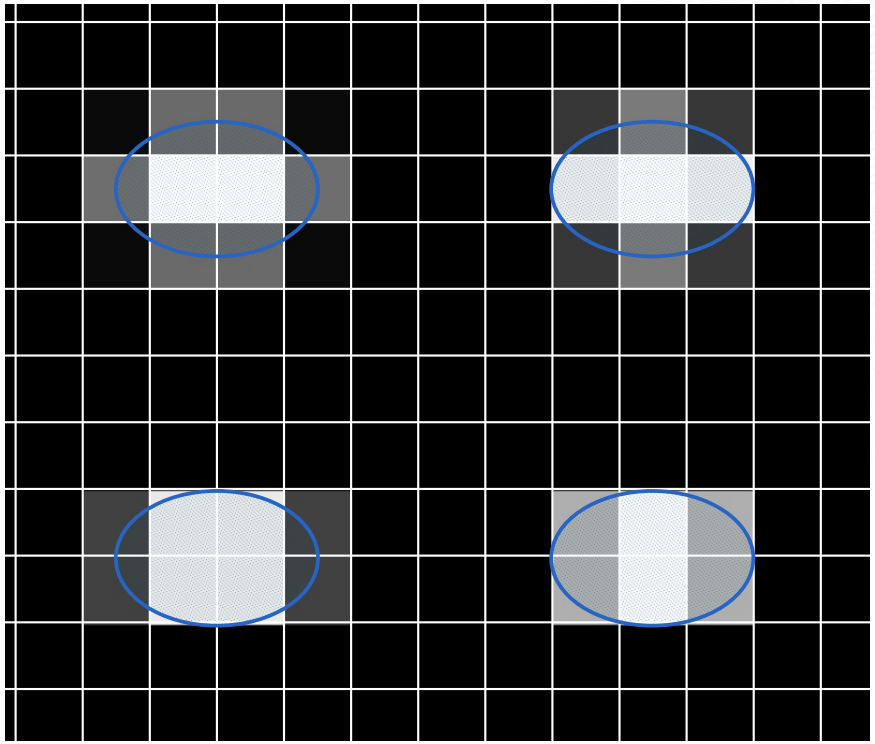
Different Pixel Alignment of the Same Shapes



Input Mask Contour

Abhishek Shendre, et al, “Leaping into the Curvy World with GPU-Accelerated O(p) Computing,”, BACUS 2024, SPIE 12751-10

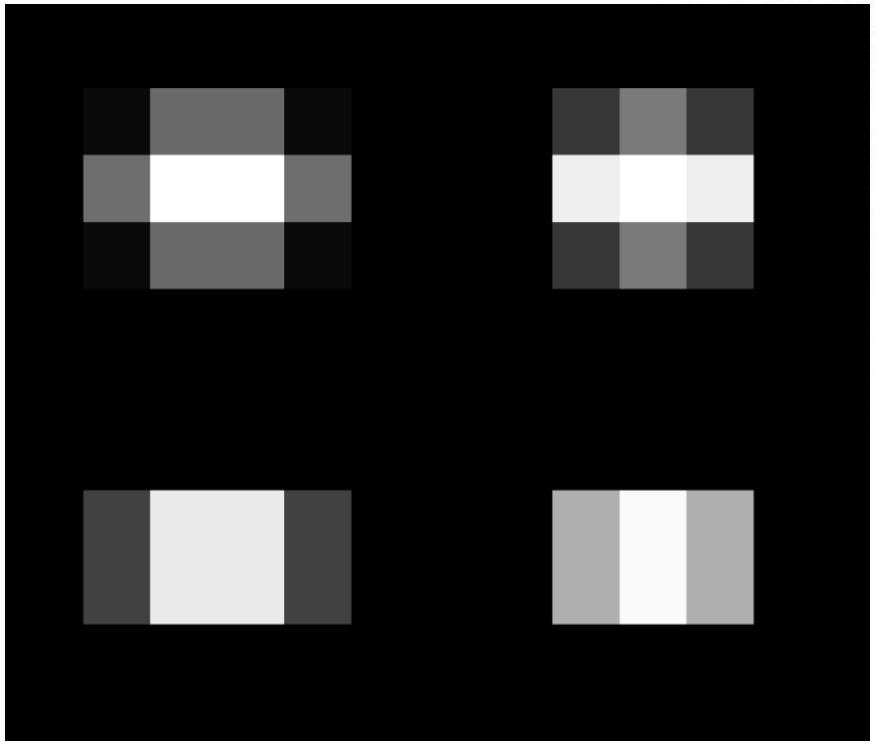
Different Pixel Alignment of the Same Shapes



Input Mask Contour

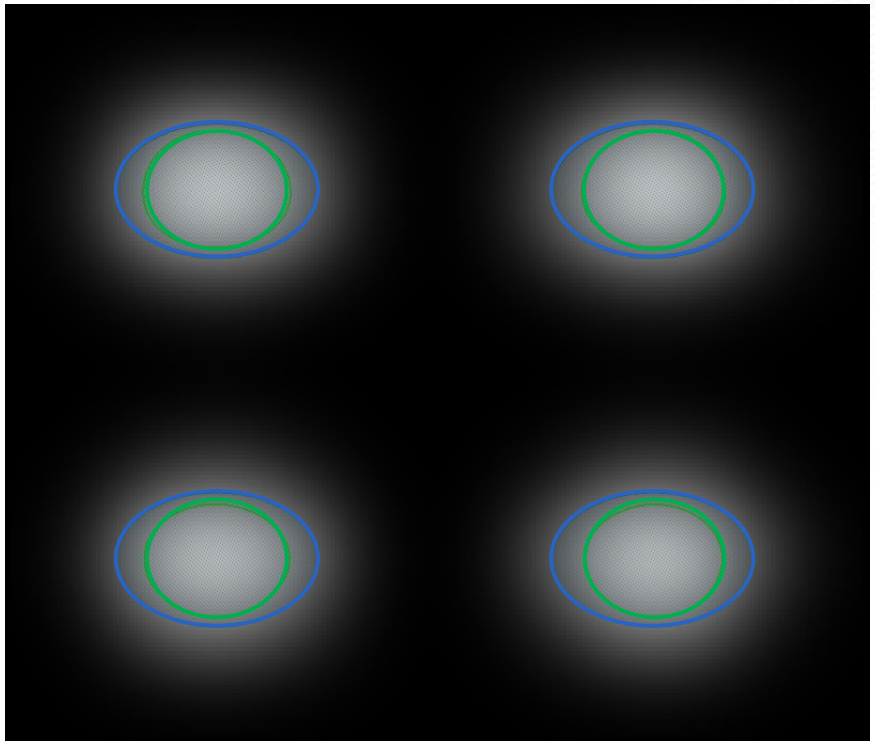
Abhishek Shendre, et al, “Leaping into the Curvy World with GPU-Accelerated O(p) Computing,”, BACUS 2024, SPIE 12751-10

Totally Different Pixel Maps Are For the Same Shape



Abhishek Shendre, et al, “Leaping into the Curvy World with GPU-Accelerated O(p) Computing,”, BACUS 2024, SPIE 12751-10

Small Shapes and Sharper Angles Need Help

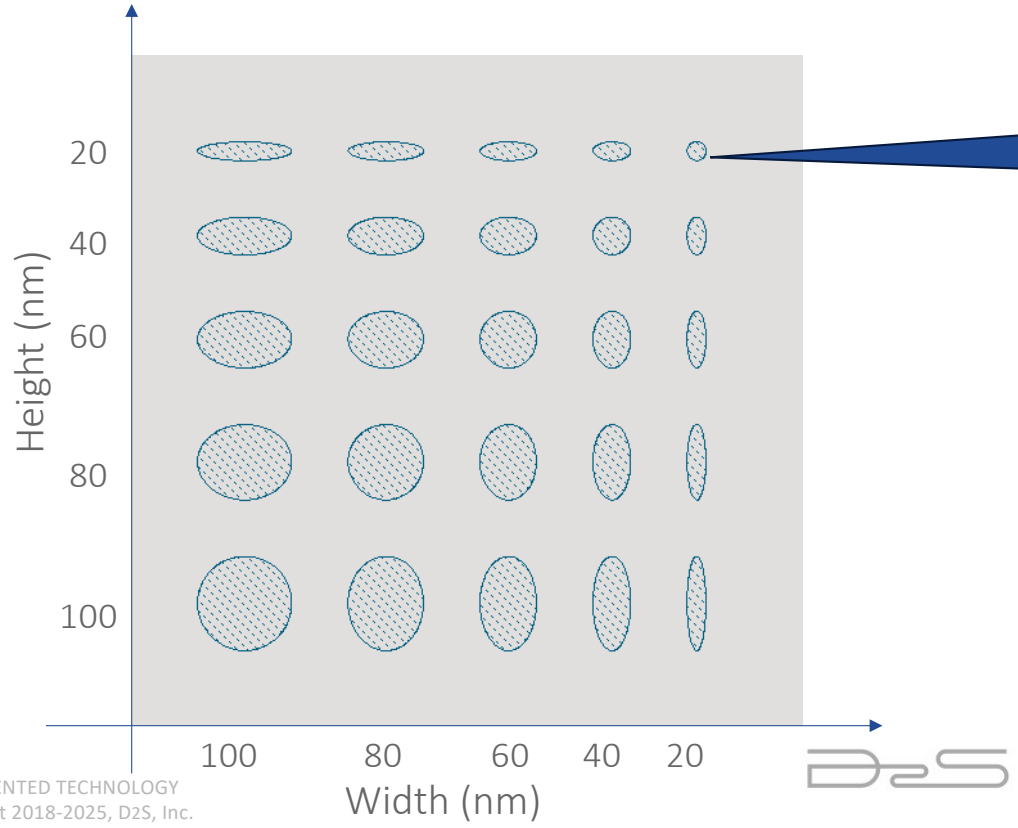


Input Mask Contour

Simulated Mask Contour

Abhishek Shendre, et al, “Leaping into the Curvy World with GPU-Accelerated O(p) Computing,”, BACUS 2024, SPIE 12751-10

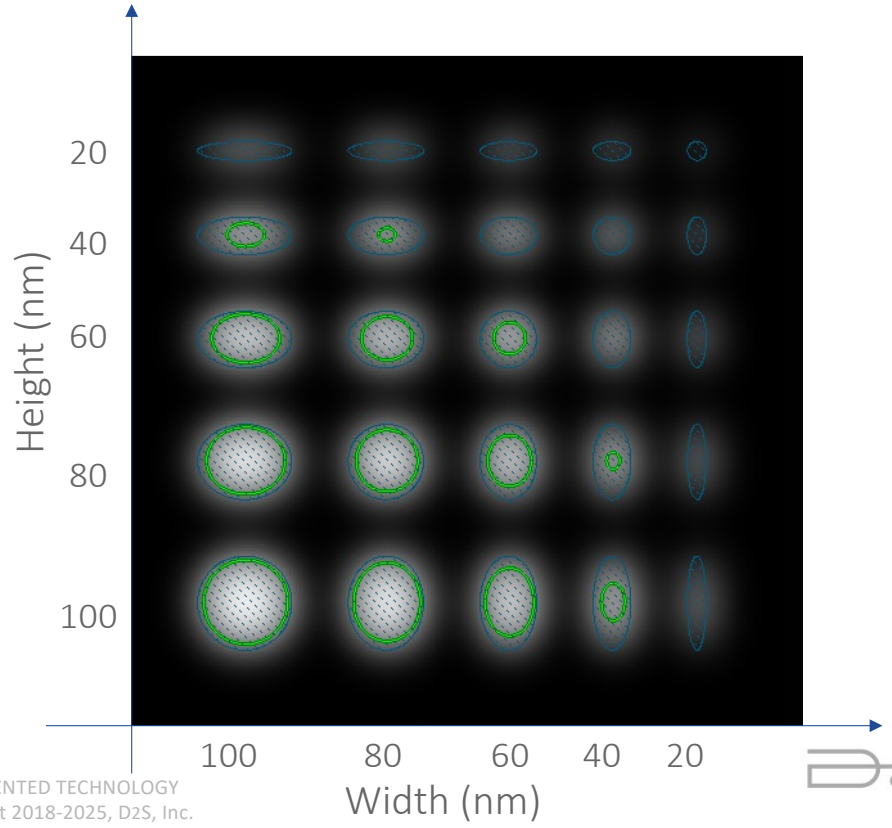
How Small/Sharp Can We Go?



Is this practical?

Abhishek Shendre, et al, "Leaping into the Curvy World with GPU-Accelerated O(p) Computing,", BACUS 2024, SPIE 12751-10

Very Small Shapes May Not Resolve

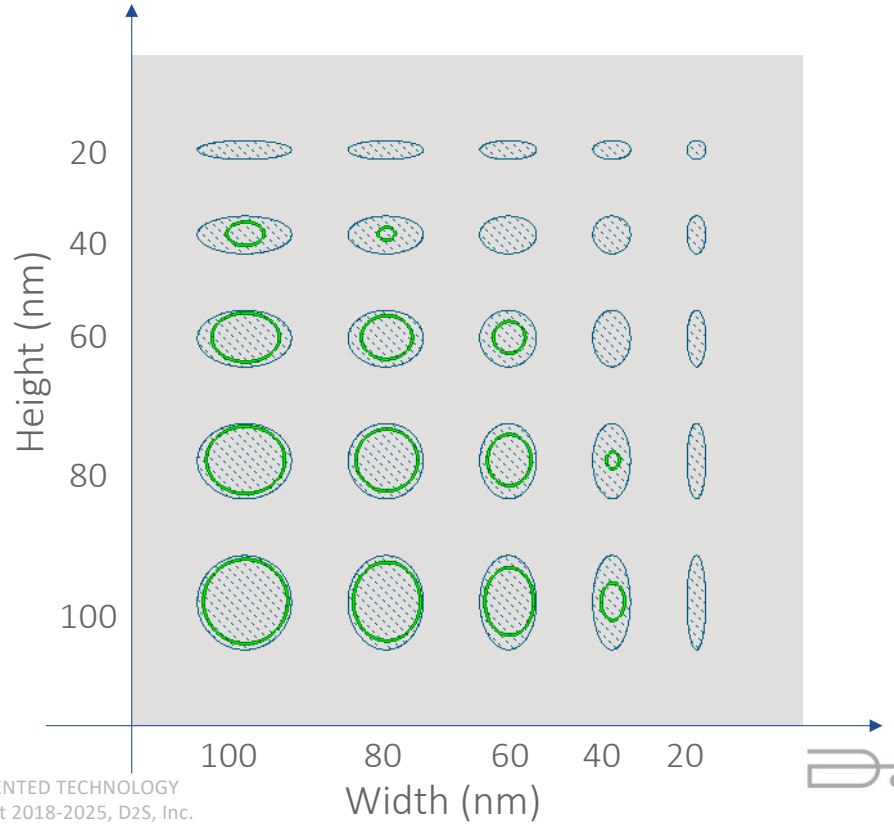


Simulated Mask Contour

Input Mask Contour

Abhishek Shendre, et al, "Leaping into the Curvy World with GPU-Accelerated O(p) Computing,", BACUS 2024, SPIE 12751-10

We Need Mask Rules to Check Manufacturability



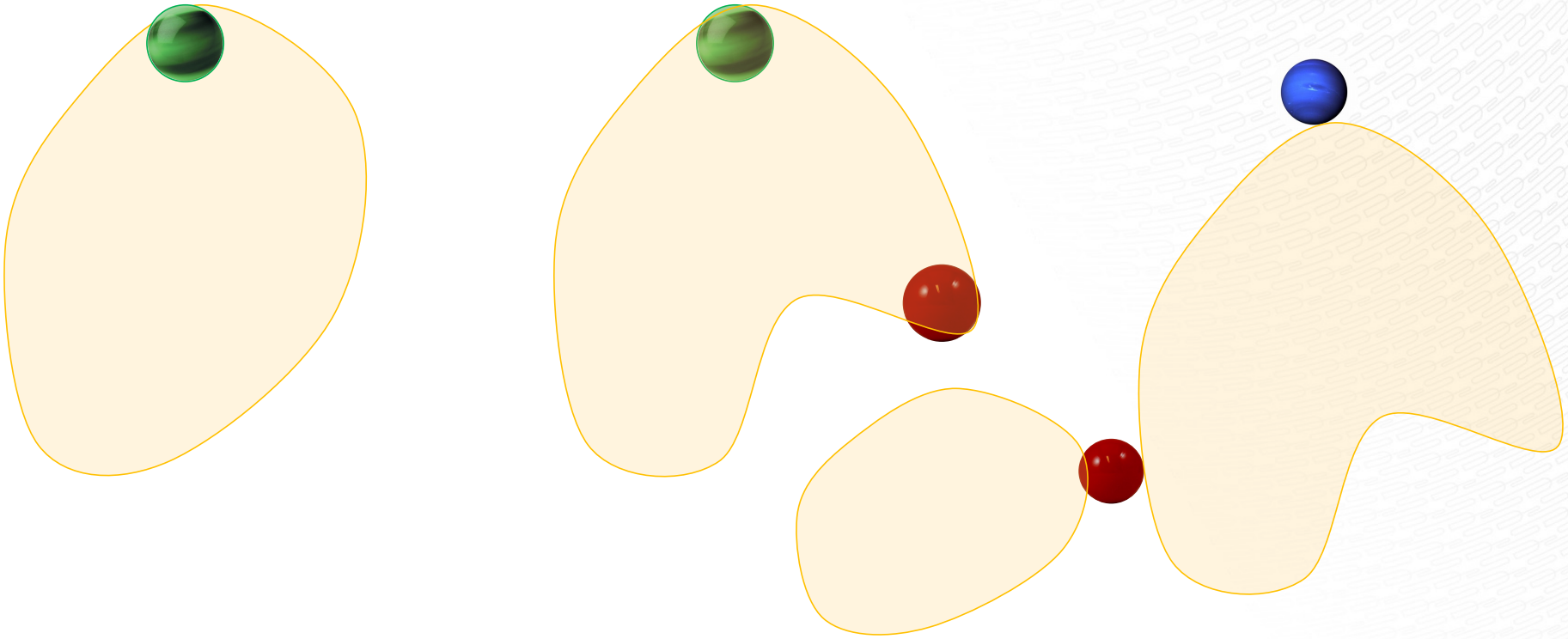
Simulated Mask Contour

Input Mask Contour

Abhishek Shendre, et al, "Leaping into the Curvy World with GPU-Accelerated O(p) Computing,", BACUS 2024, SPIE 12751-10

Curvilinear Mask Rules Need to Be a Little Different

Rolling Balls for minimum Curvature, CD, Space, and Area



Multibeam Mask Writers Enabled Curvy Masks

Curvy Masks Enabled Curvy ILT

GPU-Acceleration with $O(p)$ Solves Software Infrastructure

Full-chip curvy designs are now manufacturable

Curvy ILT enables Curvy Design

Multibeam Mask Writers Enabled Curvy Masks

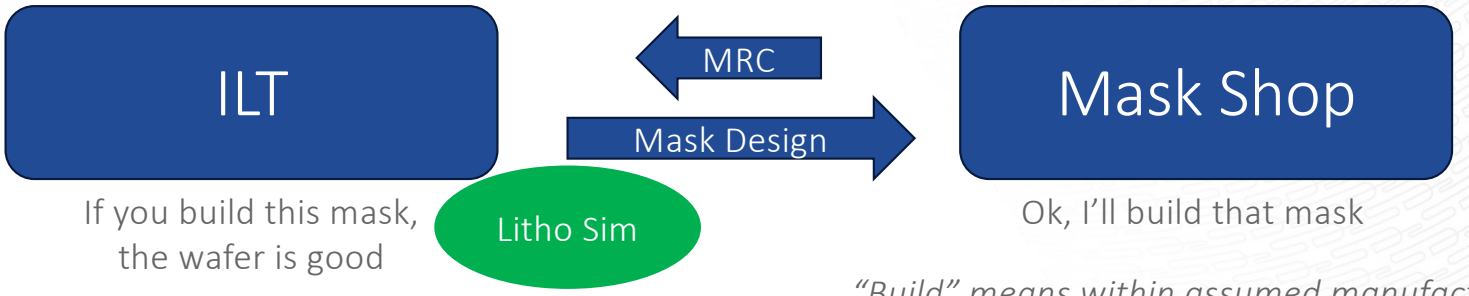
Curvy Masks Enabled Curvy ILT

GPU-Acceleration with $O(p)$ Solves Software Infrastructure

Full-chip curvy designs are now manufacturable

Wafer Simulated to the Manufactured Mask

Exactly, if ILT outputs Manufacturable Mask Shapes

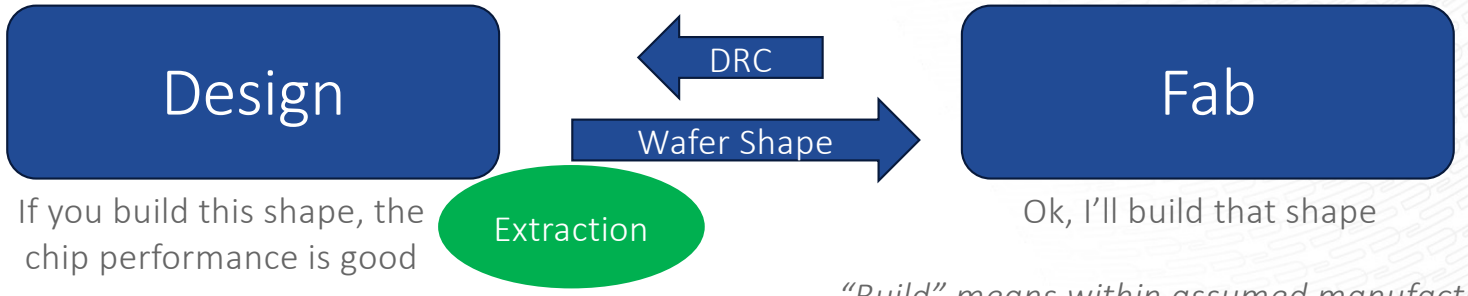


"Build" means within assumed manufacturing variation

- Wafer quality on the average is better
  - Because mask shape is exactly what ILT simulated
- Wafer variation is reduced because mask variation is reduced
- And because curvilinear ILT has much better process windows

Exactly the Same Will be True with Curvy Design

Substantially reduce timing margin by getting what you assumed

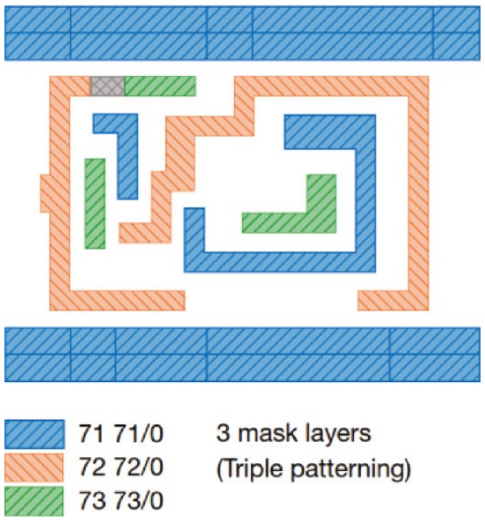


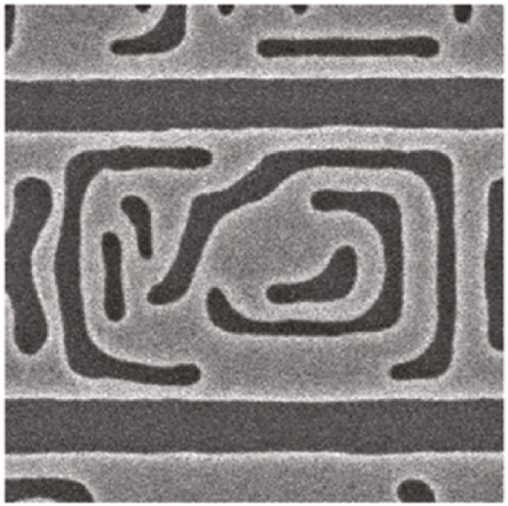
"Build" means within assumed manufacturing variation

- Manufacturing should restrict curvy design to manufacturable curvy
- Designers assume some uniform deformation of Manhattan design today
  - Parasitic extraction uses some rule-based guess of uniform deformations
  - But reality is per-instance and environment-specific deformation

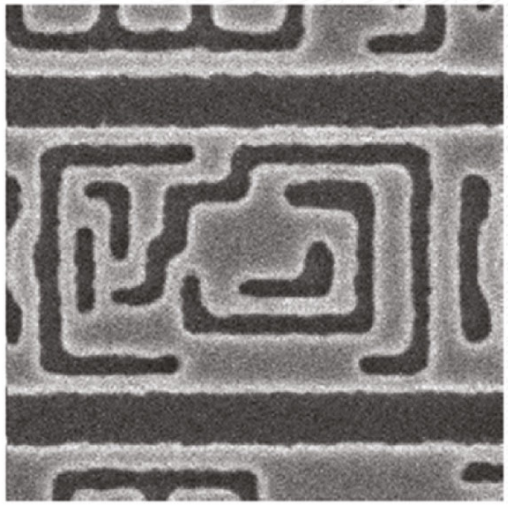
Don’t Ask for the Impossible and then Guess How Far Off

Ask for what can be manufactured and get it





193i Triple Patterning



EUV Single Patterning

From imec
Source: “Next-generation lithography – an outlook on EUV projection and nanoimprint”, Jan van Schoot and Helmut Schift, June 8, 2017, de Gruyter, Advanced Optical Technologies, 2017, 6(3-4): 159-162, DOI 10.1515/aot-2017-0040

21 years in Physical Design EDA; 21 years in Manufacturing

I'm a hybrid…

1979 AI Student BS, MS @MIT Co-op in DA A* router @Honeywell

1982 DA MTS @Trilogy

1984 Founder/ MTS @Tangent

1986 Product Mgr Tancell: First commercial system to have timing assurance and ATG

1987 VP Eng. Tangate: First commercial over-the-cell P&R system LEF/DEF ECO

1991 VP, CE DF II Rep for CFI @Cadence (acquisition)

1993 @Pure

1997 @Simplex

1999 Fire & Ice QX First fast P&R extraction

2001 X Architecture announced

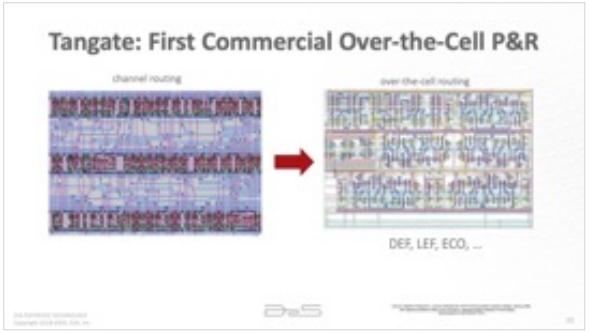
2002 MAD & DAM DFM & CTO @ Cadence (acquisition)

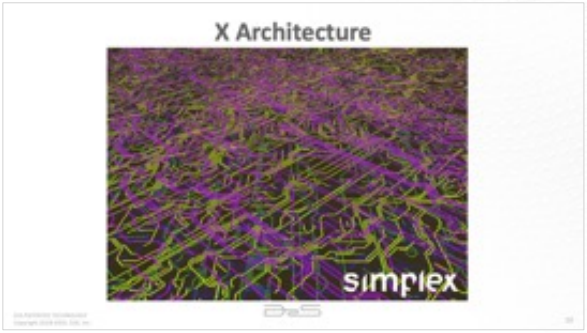
2006 D2S founded (spin out from Cadence)

2009 TrueMask® MDP First GPU-Accelerated MDP

2019 TrueMask® ILT Industry's First Full-Chip Curvy ILT/OPC @SPIE AL

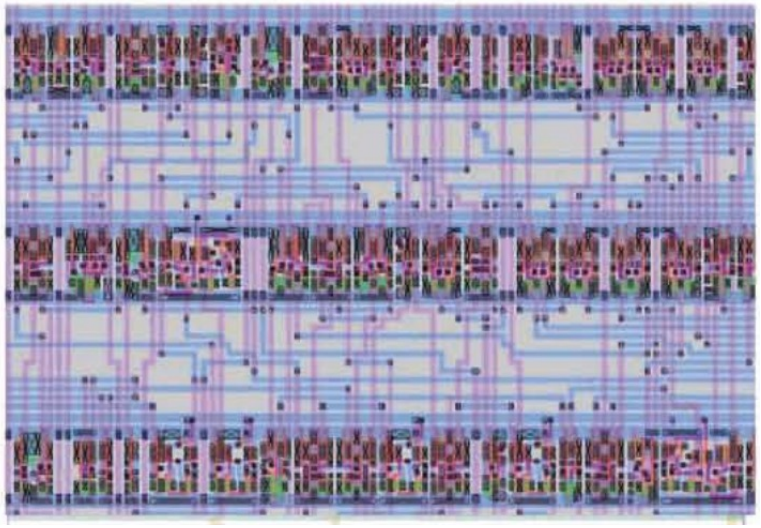
2025 Curvy Mask Solution (PLDC) from D2S Awarded Best Poster to Tekscend and Best Paper to Micron @PhotoMask Japan



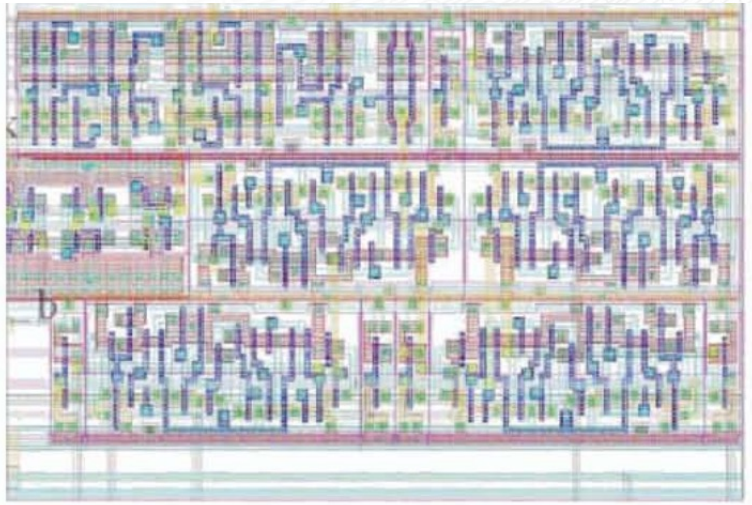


Tangate: First Commercial Over-the-Cell P&R

channel routing

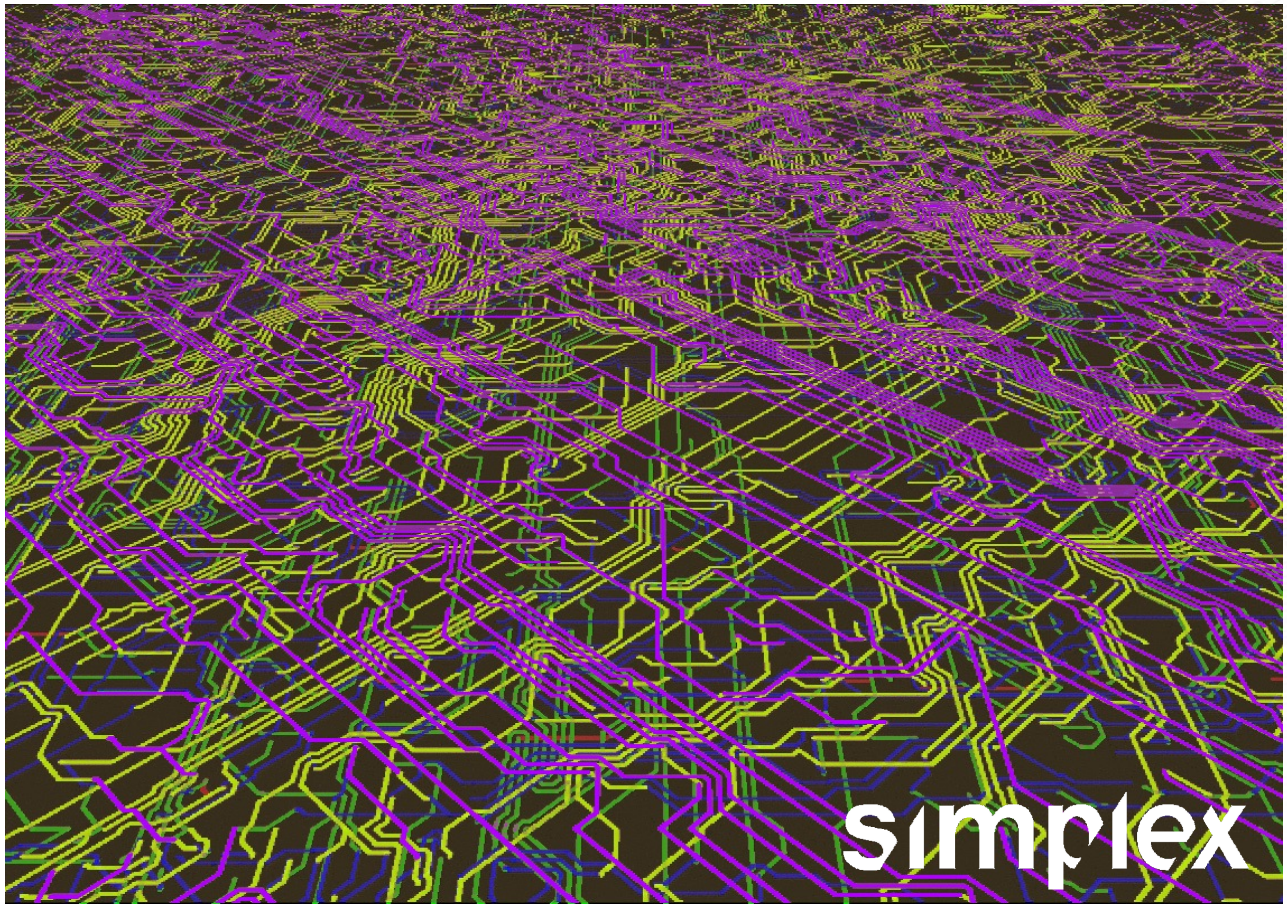


over-the-cell routing



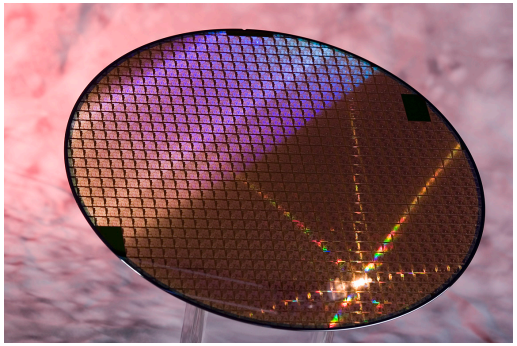
DEF, LEF, ECO, …

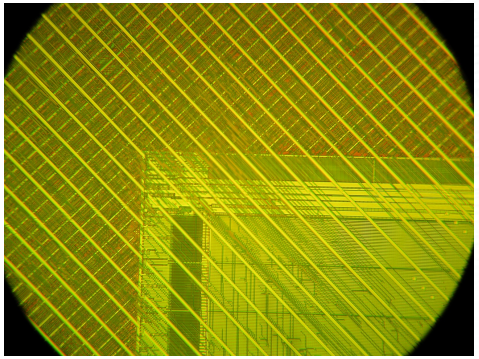
X Architecture

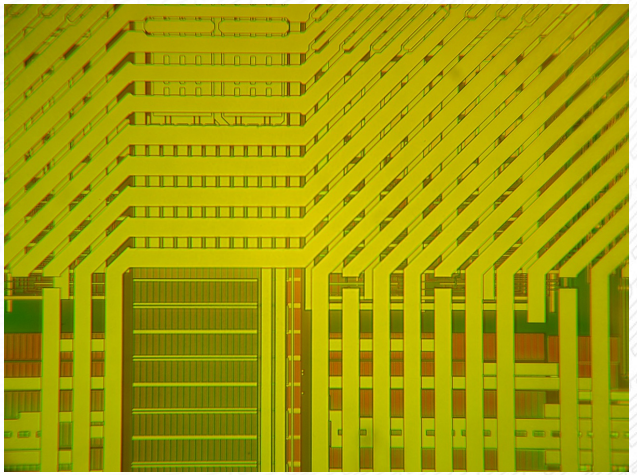


30% Wire Length Reduction from X By Many Customers

Curvy design is a superset of X Architecture





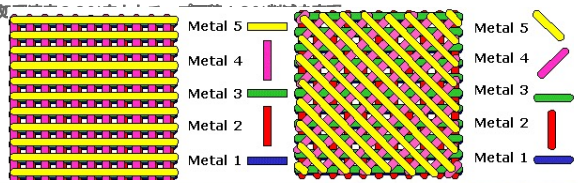


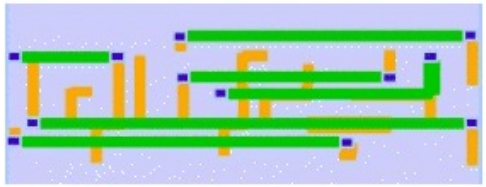
20% Faster Processing Time + 10% Area Reduction

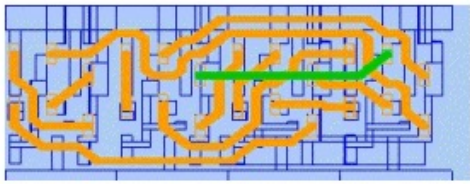
斜め配線が可能な設計手法「X　Ａｒｃｈｉｔｅｃｔｕｒｅ」による初のＬＳＩ設計について

2002年2月6日

従来手法の設計に比べ







TOSHIBA

EDN

NEWS NEWS ARCHIVE

Agere Leverages X Architecture in 90nm Mobile Chip

EDN JUNE 28, 2006 BY EDN STAFF

Print PDF Email COMMENTS 0

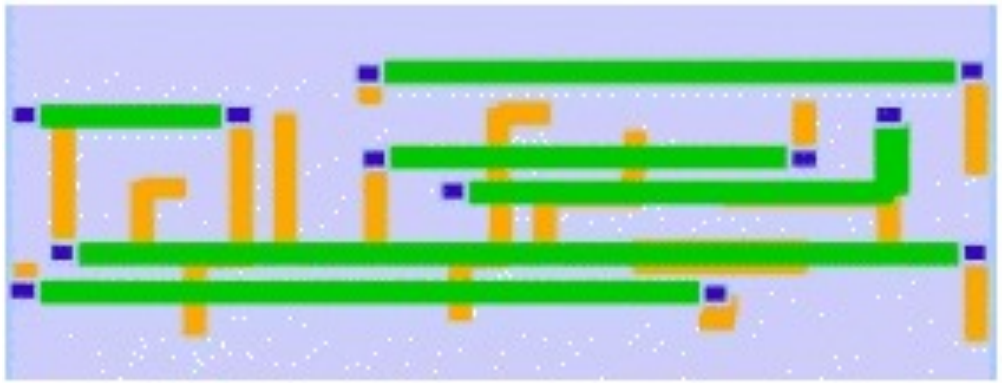
X Facts from 16 production chips

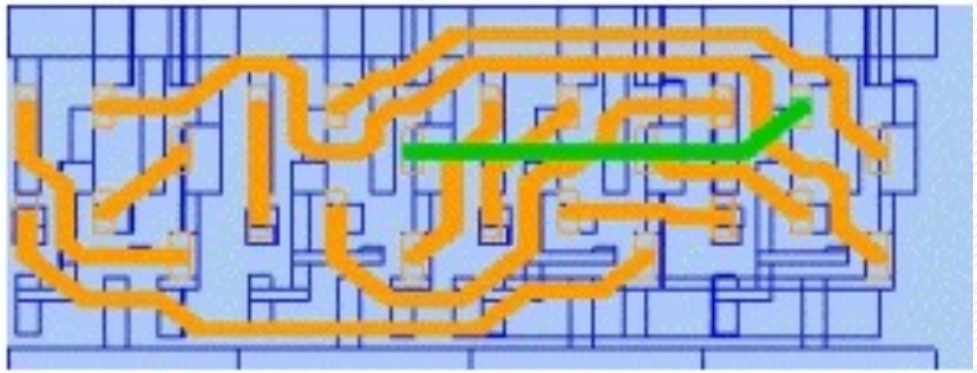
-30% wirelength	-10% area
-40% vias	Reduce 1 layer pair
+20% performance	Faster design cycles

D2S

Toshiba Used X Inside Standard Cells

Using X Architecture both for intra- and inter-connect





斜め配線が可能な設計手法「Ｘ　Ａｒｃｈｉｔｅｃｔｕｒｅ」による初のＬＳＩ設計について

2002年2月6日

従来手法の設計に比べ処理速度２０％向上とチップ面積１０％削減を実現

TOSHIBA

D2S

2025-2035

Litho Scaling is Almost Over: Devices are Going 3D

Power (and clock?) is Going to Backside

Even more interconnect limited than now

Interconnect in M2 and up can go any direction

Curvy routing is the answer

IMEC Has Been Publishing on Curvy Design

imec

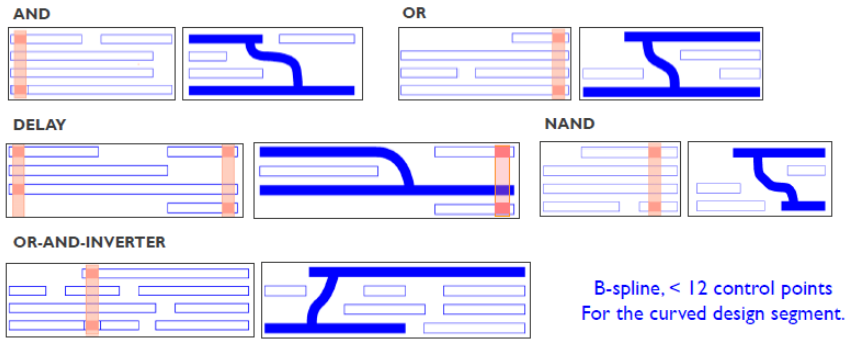
MANUFACTURING-FRIENDLY CURVILINEAR STANDARD CELL DESIGN

RYOUNG-HAN KIM, APOORVA OAK, YASSER SHERAZI, GIOELE MIRABELLI, SOOBIN HWANG, KIHO YANG, HSINLAN CHANG

PUBLIC

"PARTIAL USE" IN DESIGN

VARIOUS FORMS WHILE SATISFYING EXISTING MANUFACTURING ENVIRONMENTS



B-spline, < 12 control points
For the curved design segment.

"EDA qualified" design for near-future adoption

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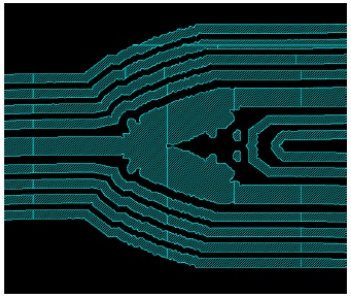
ULTIMATELY – "FREE-FORM USE" IN LOGIC DESIGN

ULTIMATE USE CASE



Inverse photonics design for illustration purpose.

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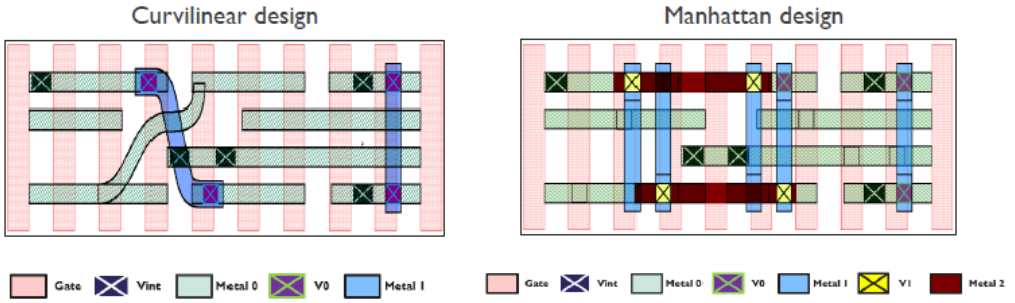
INTRA-CELL ROUTING FOR 2-TO-1 MULTIPLEXER



- Maintaining k1 as a key optimization method.
- Shorter path – Potential Resistivity (performance) benefit
- Reduction in number of layers – Manufacturability & cost benefit

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D2S

REDUCTION IN METAL LENGTH, #VIAS

28% Area Reduction for Flip-Flops

12-30% Metal Length (=Capacitance) Reduction

Number of vias in other cells reduced from 2 to 0

Number of vias in FF cells reduced from 30 to 15

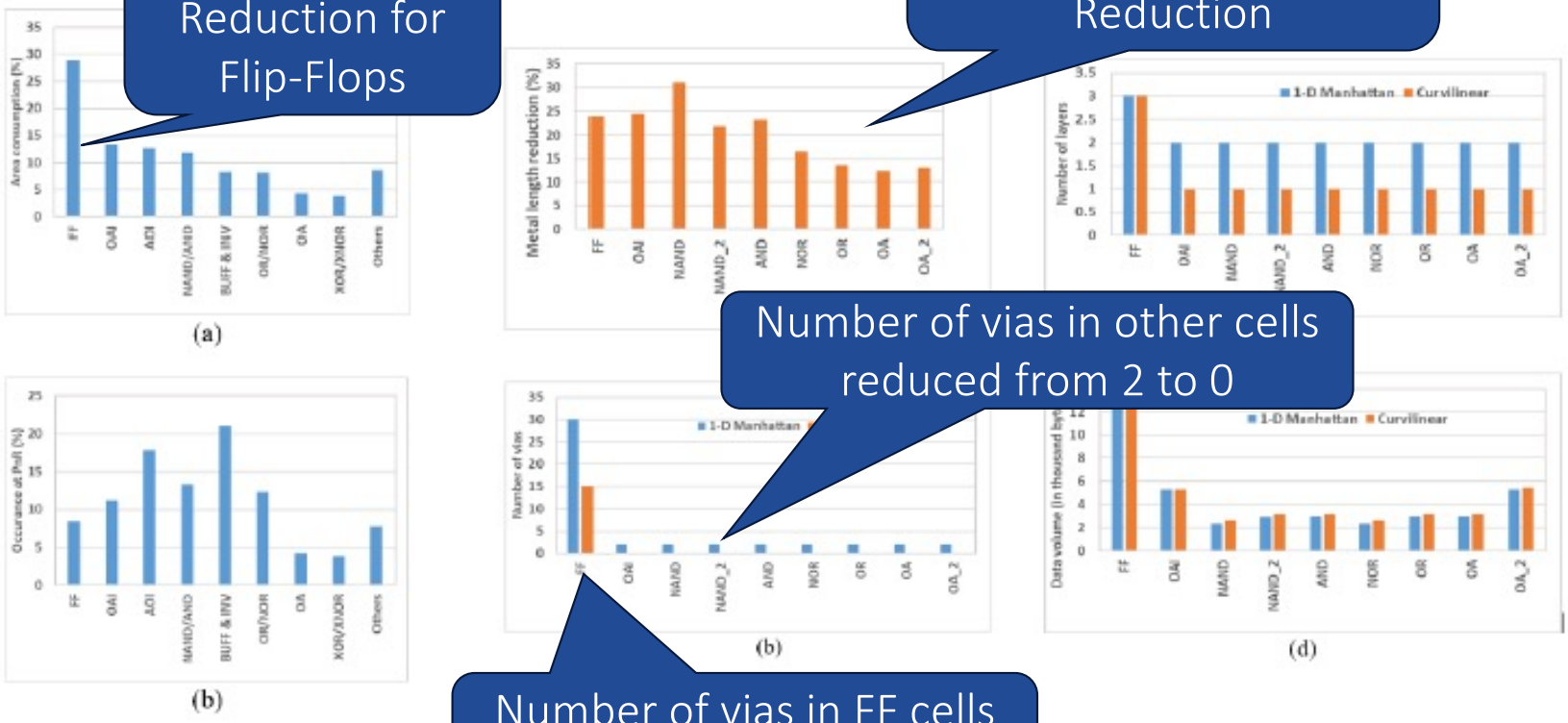

Fig. 8. Standard cells utilization as shown … area consumption (%). (b) Occurrence afte… Kim et al. in *IEEE Transactions on Semiconductor …facturing*, doi: 10.1109/TSM.2024.3362900.

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D2S

Steve Teig, Amazon's VP and Distinguished Engineer, designer of Perceive low-power AI chip, says:

Curvy is a transformative P&R technology

- Simultaneously achieve the following benefits:

Goal	Performance	Total Power		Area	Wirelength	Vias	Perf / W
Balance	+25%	-20-25%		-10%	-30-45%	-40-50%	+50-60%
	+30-35% for chiplets	-15% dynamic	-25-30% leakage	-20-25% for chiplets			

- Individually achieve the following benefits:

Goal	Performance	Total Power	Area	Perf / W
Max Performance	+40-43%	+10-15%	-5-7%	+25-30%
Max Power Savings	0%	-40-45%	-8-10%	+40-45%
Max Area Reduction	+15-18%	-15-20%	-10-14%	+35-40%
Max Efficiency	+20-25%	-25-30%	-8-10%	+65-75%

- Improved yield and reliability: 40% fewer vias, lower current density, reduced electromigration
- Improved timing closure

Get What You Ask For

By asking for manufacturable shapes,

It will be manufactured as you litho simulated/extracted,

and more reliably

The BACUS Community Enables All This!

Questions?